A 6.6-μW Wheatstone-Bridge Temperature Sensor for Biomedical Applications

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***Abstract*—This letter presents a compact, energy-efficient, and low-power Wheatstone-bridge temperature sensor for biomedical applications. To maximize sensitivity and reduce power dissipation, the sensor employs a high-resistance (600 kΩ) bridge that consists of resistors with positive (silicided-poly) and negative (*n*-poly) temperature coefficients. Resistor spread is then mitigated by trimming the *n*-poly arms with a 12-bit DAC, which consists of a 5-bit series DAC whose LSB is trimmed by a 7-bit PWM generator. The bridge is readout by a second-order delta–sigma modulator, which dynamically balances the bridge by tuning the resistance of the silicided-poly arms via a 1-bit series DAC. As a result, the modulator's bitstream average is an accurate and near-linear function of temperature, which does not require further correction in the digital domain. Fabricated in a 180-nm CMOS technology, the sensor occupies 0.12 mm^2. After a 1-point trim, it achieves +0.2 °C/−0.1 °C (3σ) inaccuracy in a ±10 °C range around body temperature (37.5 °C). It consumes 6.6 μW from a 1.6-V supply, and achieves 200-μK resolution in a 40-ms conversion time, which corresponds to a state-of-the-art resolution FoM of 11 fJ·K^2. Duty cycling the sensor results in even lower average power: 700 nW at 10 conversions/s.**

***Index Terms*—Biomedical, energy efficiency, low power, temperature sensor, trimming.**

I. Introduction

In wearable/implantable biomedical applications, body temperature (∼37.5 °C) must often be measured accurately, e.g., with errors less than 0.1 °C from 39.0 °C to 41.0 °C, and less than 0.2 °C from 35.8 °C to 41.0 °C [1]. This requires temperature sensors with sufficient resolution (< 40 mK) in a short conversion time (< 100 ms) to facilitate rapid, and thus low cost, calibration. Furthermore, since biomedical devices are typically powered by small thin-film batteries, their sensors should also have high-energy efficiency and low-power dissipation. Last but not least, such sensors should be robust to supply and clock reference variations, as a stable supply/clock is not always available in biomedical environments.

BJT- or MOS-based temperature sensors are often used in biomedical applications due to their low-power dissipation (< 2 μW) and high resolution [2]–[4]. Wheatstone-bridge (WhB) sensors achieve state-of-the-art energy efficiency [5], [6], but typically dissipate more power (> 50 μW) and are quite nonlinear, requiring a complex digital backend to perform polynomial linearization. Some resistor-based sensors [7], [8] dissipate much less power (< 0.1 μW), however, they are much less energy efficient, and their limited resolution (> 300 mK) makes them unsuitable for use in biomedical applications.

This letter presents a low-power WhB sensor that meets biomedical requirements while maintaining high energy efficiency. After a PWM-based 1-point trim, it achieves an inaccuracy of +0.2 °C/−0.1 °C (3σ) over a ±10 °C range centered on 37.5 °C. The use of PWM-based trimming obviates the need for a complex digital backend that implements a high-order linearizing polynomial and a correlated gain/offset trim [6]. It is also quite energy efficient, achieving 200-μK resolution in a 40-ms conversion time while dissipating 6.6 μW, which corresponds to a state-of-the-art resolution FoM of 11 fJ·K^2. A power-down mode allows its average power to be significantly reduced, by duty cycling, to ∼700 nW at 10 conversions/s.

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II. Wheatstone Bridge and Sensor Readout

A. Wheatstone Bridge and Series RDAC

To maximize its sensitivity, the WhB sensor employs resistors with opposite temperature coefficients (TCs): silicided poly resistors (R_p) and *n*-poly resistors (R_n). Since the bridge dominates both the sensor's area and power dissipation, there is a tradeoff between these two important parameters. With $R_n \approx R_p \approx 600$ kΩ, i.e., ∼ 6× more than in [5] and [6], the WhB consumes ∼ 4.3 μW from a 1.6-V supply, and occupies 0.06 mm^2.

In [5] and [6], the output of a WhB is digitized by a continuous-time delta–sigma modulator ($CT\Delta\Sigma M$), which uses a parallel *n*-poly DAC ($R_{n\mathrm{DAC}}$) to dynamically balance the bridge [Fig. 1(a)]. In steady state, the $CT\Delta\Sigma M$'s bitstream (BS) average μ can be expressed as

$$\mu = R_{n\mathrm{DAC}}/R_n - R_{n\mathrm{DAC}}/R_p. \tag{1}$$

Since $R_{n\mathrm{DAC}}$ and R_n are both *n*-poly resistors, the first term is a constant. However, since the absolute TC of R_p (0.29%/°C) is larger than that of R_n (−0.15%/°C), the second term is proportional to $1/T$ and is thus rather nonlinear. Together with the resistors' higher-order TCs, this results in a nonlinearity of ∼ 0.3 °C over the desired range (±10 °C range around 37.5 °C), which would then necessitate the use of polynomial nonlinearity correction [5], [6].

This nonlinearity can be mitigated by realizing the DAC with R_p resistors [Fig. 1(b)], in which case, μ can be expressed as

$$\mu = R_{p\mathrm{DAC}}/R_p - R_{p\mathrm{DAC}}/R_n. \tag{2}$$

This reduces the nonlinearity to ∼ 0.1 °C over the same temperature range, obviating the need for digital linearization.

Since the desired temperature range is small (20 °C), the resistance change in the R_n branch will also be small, and a large parallel resistor ($R_{p\mathrm{DAC}} \approx 18 \cdot R_p$) is required to balance the bridge. To save area, a series DAC is used [9], which requires a much smaller ($R_{p\mathrm{DAC}} \approx R_p/18$) resistor [Fig. 1(b), middle].

In this case, μ can be expressed as

$$\mu = (2k+1) - (2k+2) \cdot R_p/R_n \tag{3}$$

where $k = R_p/R_{p\mathrm{DAC}}$. As in (2), its nonlinearity is also determined by the $R_{p\mathrm{DAC}}/R_n$ and so remains the same.

B. PWM-Assisted Trim

To compensate for process spread, the R_p/R_n ratio can be adjusted by trimming the R_n branch. However, compensating for the worst-case process spread (±40%) and achieving sufficient trimming resolution (< 0.05 °C) requires a 12-bit trim DAC. To save area, this is implemented by combining a 5-bit resistor DAC (∼15 kΩ/step) with a 7-bit PWM DAC. The former ensures efficient use of the modulator's dynamic range, while the latter provides sufficient resolution. As shown in Fig. 2, the resistor DAC is implemented with 31 series resistors, and the PWM trim is implemented by duty cycling an extra series resistor at $F_{\mathrm{PWM}} = F_S/128$, where F_S (=32 kHz) is the sampling frequency of the modulator. To ensure a constant switch on-resistance, a dummy switch controlled by the inverse of the PWM signal (!PWM) is added in series with the duty-cycled resistor. Although quite area efficient, the PWM trim adds a small ac component to the output current of the bridge I_{err}, which uses up to ∼20% of the modulator's input dynamic range.

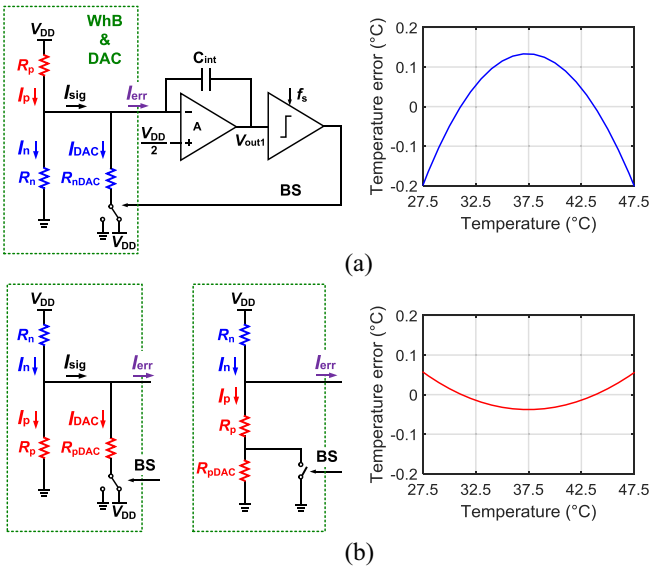

Fig. 1. Simulated nonlinearity of a WhB sensor (a) with a parallel R_n DAC and (b) with a parallel/series R_p DAC.

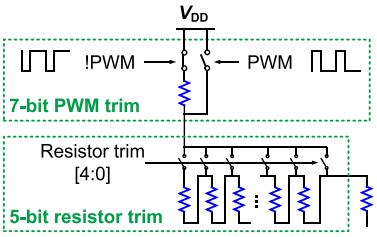

Fig. 2. Hybrid R_n trim based on resistor segmentation and PWM.

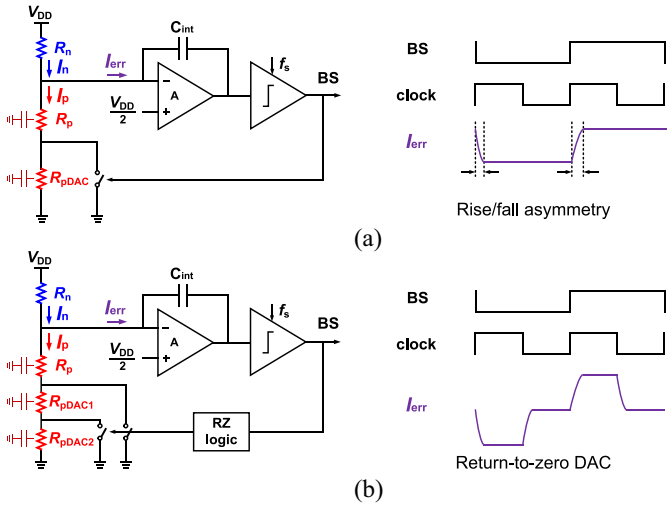

Fig. 3. (a) Rise/fall asymmetry when using an NRZ DAC. (b) RZ DAC achieved by splitting $R_{p\mathrm{DAC}}$.

C. Return-to-Zero DAC and DSM Readout

One drawback of a series R_p DAC is that it modulates the resistance of the R_p branches. Due to their parasitic capacitances, the resulting rise/fall times of I_{err} (~ 0.5 μs) are quite significant when compared to the clock period (31.25 μs). Using non-return-to-zero (NRZ) DAC pulses will then cause intersymbol interference (ISI), and degrade the modulator's noise floor. To mitigate this, a return-to-zero (RZ) DAC is implemented by splitting $R_{p\mathrm{DAC}}$ in two and returning to the resulting middle level after a half clock period, as shown in Fig. 3(b).

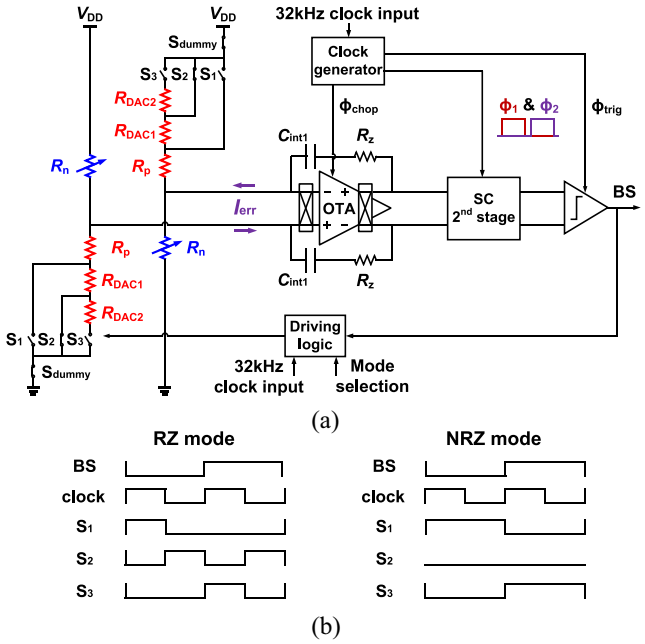

Fig. 4. (a) Simplified sensor block diagram. (b) DAC switching scheme under RZ or NRZ mode.

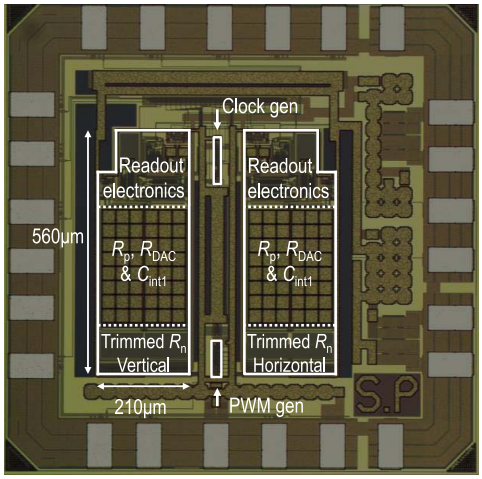

Fig. 5. Die photograph of the fabricated chip.

To improve the sensor's supply sensitivity, dummy switches (S_{dummy}) are also inserted in series with the DAC switches (S_1–S_3), so that there are always two series switches in both WhB branches, which cancels the effect of the voltage dependency of switch on-resistance.

The sensor's system block diagram is shown in Fig. 4(a). To achieve high resolution, the bridge is read out by a second-order DSM. As in [5], the first stage is built around a current-reuse OTA, which employs high threshold voltage (high-V_T) input transistors to maximize its output range, and chopping to suppress its $1/f$ noise [5]. The second stage employs another current-reuse OTA and area-efficient switched-capacitor filter [6].

Two extra operating modes have also been implemented. First, to test the effectiveness of the RZ DAC, an NRZ DAC can be implemented by modifying the timing of the signals that drive S_1–S_3, as shown in Fig. 4(b). Second, to implement a power-down mode, the WhB is disconnected from the supply by turning S_{dummy} off. The amplifiers are also switched off by shorting the gates of their pMOS/nMOS tail-current sources to V_{DD}/Gnd. For fast startup, capacitors precharged to Gnd/V_{DD} can be used to restore their gate voltages within one clock cycle [8].

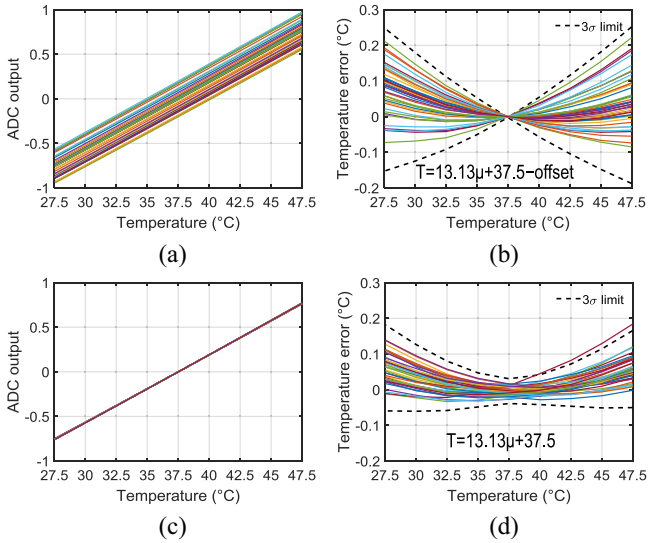

Fig. 6. (a) Measured output of the ceramic-packaged sensors after resistor trim. (b) Inaccuracy after digital offset trim. (c) Measured output after PWM trim. (d) Inaccuracy after PWM trim without post-processing.

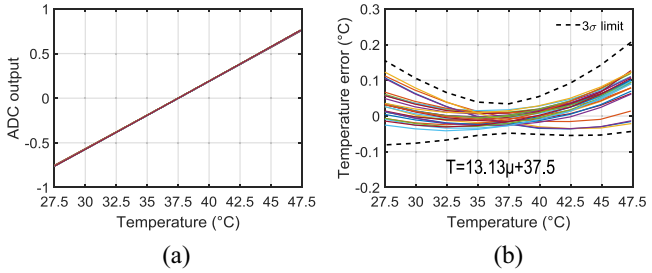

Fig. 7. (a) Measured output of plastic-packaged sensors after PWM trim. (b) Inaccuracy after PWM trim.

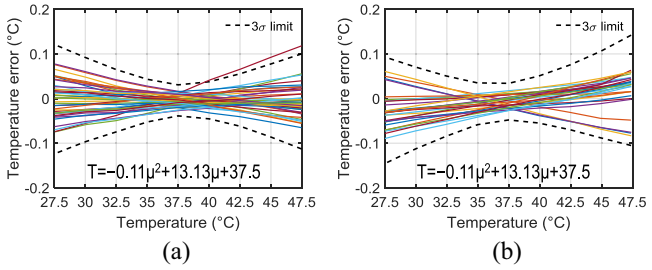

Fig. 8. Temperature inaccuracy with a quadratic master curve of (a) ceramic-packaged sensors and (b) plastic-packaged sensors.

III. Measurement Results

As shown in Fig. 5, two sensors are fabricated on the same die in a standard 0.18-μm CMOS process, allowing ambient temperature drift to be canceled by differential measurements [6]. They share the same clock/PWM generation circuit (0.003 mm^2), and for flexibility, their decimation filters (sinc^2) are off-chip. The large first stage integration capacitors C_{int1} (MIM, 40 pF) are located above the WhB (0.072 mm^2), while the trimming circuits occupy 0.007 mm^2. At F_S = 32 kHz, each sensor consumes 6.6 μW (4.2-μW bridge, 2.1-μW analog, and 0.3-μW digital) from a 1.6-V supply, and occupies 0.12 mm^2.

A. Trimming and Accuracy

The sensors (21 ceramic-packaged samples from one wafer) were characterized from 27.5 °C to 47.5 °C in a temperature-controlled oven. Without trimming, the sensor's inaccuracy is about 10 °C. After a 5-bit resistor trim at 37.5 °C, the residual spread relative to a linear master curve is about ±2.5 °C [Fig. 6(a)]. This can be reduced to ±0.25 °C (3σ) by applying a digital offset trim [Fig. 6(b)].

As indicated by (3), some of the remaining spread is caused by the residual error in the ratio R_p/R_n, which causes sensitivity variations that cannot be eliminated by the aforementioned offset trim. By trimming R_p/R_n(5-bit resistor trim + 7-bit PWM trim), this error is greatly suppressed, as shown in Fig. 6(c). Despite the residual trimming error at 37.5 °C, the residual spread is then below +0.2 °C/−0.1 °C (3σ) without any additional post-processing [Fig. 6(d)].

To investigate the effects of packaging stress, 14 plastic-packaged chips from the same wafer were also characterized. This causes a systematic sensitivity error and increased spread. Using the linear master curve obtained from the ceramic-packaged chips results in +0.25/−0.1 °C (3σ), as shown in Fig. 7.

Even better accuracy can be achieved by using a quadratic master curve at the expense of a more complex digital backend. This results in a residual spread of below ±0.15 °C (3σ) for both ceramic- and plastic-packaged sensors, as shown in Fig. 8.

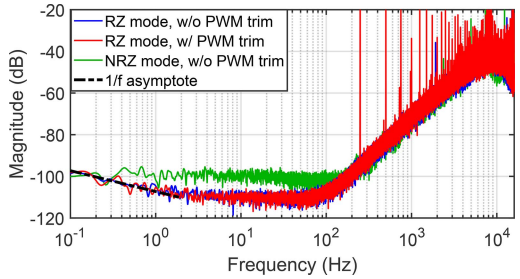

Fig. 9. Measured BS spectra with different settings.

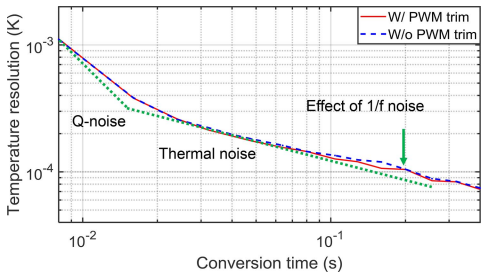

Fig. 10. Measured resolution versus conversion time with/without PWM trim.

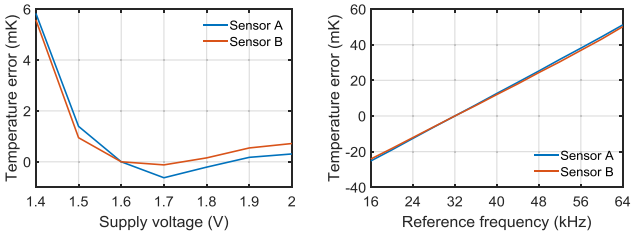

Fig. 11. (a) Supply sensitivity and (b) clock frequency sensitivity of two sensors on the same chip.

B. Resolution

FFTs of the sensor's BS outputs are shown in Fig. 9. As expected, the use of an NRZ DAC instead of an RZ DAC significantly degrades the modulator's noise floor (by 9 dB). Although PWM trimming does not impact the sensor's noise floor, it does introduce strong high-frequency tones. By limiting the conversion time (T_{conv}) to multiples of 8 ms, these tones can be completely filtered out by the notches of the sinc^2 decimation filter. For T_{conv} = 8 ms/40 ms, the sensor achieves 1.1 mK/200 μK (rms) resolution (Fig. 10), corresponding to resolution FoMs of 65 fJ·K^2/11 fJ·K^2.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORK

	[2]	[3]	[4]	[7]	[8]	[5]	[6]	**This work**	
Sensor type	BJT	MOS	DTMOST	Resistor	Resistor	Resistor	Resistor	**Resistor**	
CMOS Technology [nm]	180	350	160	180	65	180	180	**180**	
Area [mm^2]	0.198	0.084	0.085	0.09	0.084	0.35	0.11	**0.12**	
Temperature range	25°C to 45°C	35°C to 45°C	-40°C to 125°C	-0°C to 100°C	-10°C to 120°C	-55°C to 125°C	-55°C to 125°C	**27.5°C to 47.5°C**	
3σ inaccuracy [°C] (trimming points)	±0.2 (1)	±0.1 [a] (2)	±0.4 (1)	+1.5/-1.4 [a] (2)	+0.34/-0.29 [a] (2)	±0.12 (2)	±0.1 (2)	**+0.2/-0.1 (1)**	
Number of samples	20	3	16	18	10	19	40	**42**	
On-chip trim	No	No	No	No	No	No	No	**Yes**	
Supply voltage (V)	1.0 & 1.8	1.4 & 2.1	0.85	1.2	0.6 & 1	1.8	1.8	**1.6**	
Supply sensitivity (°C/V)	N.A.	0.3	0.45	14	1.0	0.02	0.04	**0.004**	
Power consumption [µW]	1.1	0.11	0.6	0.071	0.00035	94	55	**6.6**	
Conversion time [ms]	500	100	6	30	1000	5	8	**8**	**40**
Resolution [mK]	10	35	63	300	380	0.29	0.15	**1.1**	**0.20**
Resolution FoM [fJ·K^2] [b]	55000	13000	14100	190000	50000	40	10	**64**	**11**

[a] Min or max [b] Resolution FoM = Energy / Conversion * Resolution^2

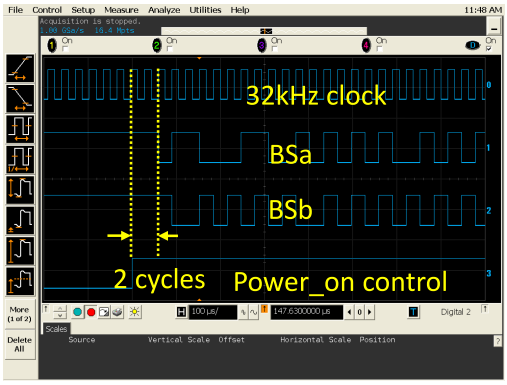

Fig. 12. Measured BS outputs of a chip around the rising edge of power-on control.

C. Supply and Clock Sensitivity

As shown in Fig. 11(a), the sensor achieves a power-supply sensitivity of only 4 mK/V from 1.5 to 2 V at 37.5 °C (box method), which is the lowest ever reported for a temperature sensor. Its output is also robust to both input clock inaccuracy (1.6 mK/kHz) and clock jitter (< 10% worse resolution with 2.2-ns cycle-to-cycle jitter), as shown in Fig. 11(b). This makes the sensor well suited for use in wearable/implantable devices which often lack stable power supplies or well-defined clocks.

D. Power-Down Mode

In the power-down mode, the sensor only draws 125 nA at 37.5 °C. As shown in Fig. 12, the sensor starts up within 2 clock cycles (62.5 μs) of the rising edge of the power-on signal, thus facilitating efficient duty cycling. At 10 conversions/s and $T_{\text{conv}} = 8$ ms, it dissipates an average power of only ~700 nW.

E. Comparison With Prior Art

Table I summarizes the performance of the proposed temperature sensor and compares it with the prior art. Compared to previous low-power designs [2]–[4], [7], [8], it achieves much higher resolution and a state-of-the-art resolution FoM. Moreover, the use of on-chip trimming means that, apart from a decimation filter, no further digital hardware, e.g., for polynomial linearization or correlated trimming, is required. In contrast, after an offset trim, the measured inaccuracy of the sensors in [6] is limited by nonlinearity and sensitivity variations, and is about −0.6 °C/+0.2 °C (3σ) over the same temperature range.

IV. CONCLUSION

A compact low-power resistor-based temperature sensor for biomedical purposes has been implemented in a standard 0.18-μm technology. It is built around a high-resistance (600 kΩ) WhB that is read out in a self-balanced manner by a continuous-time delta–sigma modulator. An appropriately designed 1-bit series DAC improves both sensor nonlinearity and chip area, while a PWM-based trim reduces sensor spread and greatly simplifies its digital back-end. The sensor occupies 0.12 mm^2 and consumes only 6.6 μW from a 1.6-V supply. Additionally, it achieves a resolution FoM of 11 fJ·K^2 and an inaccuracy of +0.2 °C/−0.1 °C (3σ) in a ±10 °C range around body temperature. These results demonstrate that the proposed sensor can serve as an energy-efficient replacement for BJT- or MOS-based temperature sensors in biomedical applications.

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