A 0.12 mm² 7.4 µW Micropower Temperature Sensor With an Inaccuracy of ±0.2°C (3σ) From −30°C to 125°C

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Abstract—This paper describes the design of a CMOS smart temperature sensor intended for RFID applications. The PNP-based sensor uses a digitally-assisted readout scheme that reduces the complexity and area of the analog circuitry and simplifies trimming. A key feature of this scheme is an energy-efficient two-step zoom ADC that combines a coarse 5-bit SAR conversion with a fine 10-bit $\Sigma\Delta$ conversion. After a single trim at 30°C, the sensor achieves an inaccuracy of ±0.2°C (3σ) from −30°C to 125°C. It also achieves a resolution of 15 mK at a conversion rate of 10 Hz. The sensor occupies only 0.12 mm² in a 0.16 µm CMOS process, and draws 4.6 µA from a 1.6 V to 2 V supply. This corresponds to a minimum power dissipation of 7.4 µW, the lowest ever reported for a precision temperature sensor.

Index Terms—SAR, sigma-delta modulation, smart sensors, temperature sensor.

I. INTRODUCTION

ENERGY efficiency and low-power operation are key requirements of battery powered systems such as wireless sensor nodes and radio frequency identification (RFID) tags. Adding temperature sensors to such systems will open up new applications in the medical, industrial, automotive and consumer fields. Such sensors, however, must be both accurate (with errors below ±1°C) and energy-efficient (operating at nano-Joule per conversion levels). They should also be *smart*, i.e. output digital data, to facilitate the flexible use of energy-efficient digital communication protocols. Lastly, they should also be low cost, which implies small chip area and, at most, a one-point (room temperature) trim.

In recent work, a number of smart temperature sensors intended for autonomous applications have been reported [1]–[6]. The sensors presented in [1]–[3] use MOSFETs as temperature sensing elements. Although they are quite energy efficient, requiring as little as 0.4 nJ/conversion [2], their inaccuracy, even after an expensive two-point trim, is still in the order of a few degrees. By contrast, the sensor in [4] is based on the parasitic

NPN transistors available in modern CMOS processes. It is energy efficient, requiring 96 nJ/conversion, but its inaccuracy, after a one-point trim, is only ±0.8°C (3σ, 9 samples) over a limited temperature range: −20°C to 30°C. Alternatively, the temperature dependency of on-chip resistors can be utilized to realize compact and energy-efficient smart sensors [5], [6]. However, since the spread of such resistors is large (20–30%) and their temperature dependence is typically nonlinear, two- or even three-point trimming is required to achieve accuracy levels comparable to transistor-based sensors [7].

Smart temperature sensors based on parasitic bipolar transistors have achieved inaccuracies of a few tenths of a degree over the military temperature range, i.e. from −55°C to 125°C, and require only a one-point trim [9]–[11]. This level of accuracy relies on the use of precision readout circuitry combined with a high resolution calibration. Therefore, $\Delta\Sigma$-ADCs have been widely used in BJT-based sensors, since they meet the low speed (typically less than 10 conversions/s), and high resolution (up to 15 bit) requirements of precision temperature sensors [8]. Moreover, the averaging nature of a $\Delta\Sigma$-ADC is well-matched to the use of dynamic error-correction techniques such as chopping and dynamic element matching (DEM) [17]. However, their power consumption often dominates the resulting sensor's total power consumption, e.g. 80% of the total power consumption in [10] is consumed by $\Delta\Sigma$-ADC.

The hardware simplicity of SAR-ADCs makes them a good alternative for ultra low-power, energy efficient applications. However, without calibration, the resolution of SAR-ADCs is limited to about 10 ∼ 12 bits. This lack of resolution, together with their sampling nature, means that such ADCs are not well-matched to the use of dynamic techniques. To realize accurate and energy-efficient smart temperature sensors, there is therefore a need for energy-efficient precision ADC architectures.

This paper presents a "zoom-ADC" architecture that maintains the resolution and accuracy of $\Delta\Sigma$-ADCs, but is much more energy efficient. It operates as follows; first, a successive-approximation algorithm is used to estimate the temperature; then, the references of a $\Delta\Sigma$-ADC are accurately adjusted to cover a small range around the estimated temperature, whereupon the exact temperature can be precisely determined. Since this range is considerably smaller than the sensor's total operating range, the $\Delta\Sigma$-ADC's resolution, and hence its conversion time, can be significantly reduced.

In the following section, the sensor's operating principle is explained in more detail. Section III is devoted to the sensor's analog front-end, while Section IV describes the zoom ADC and
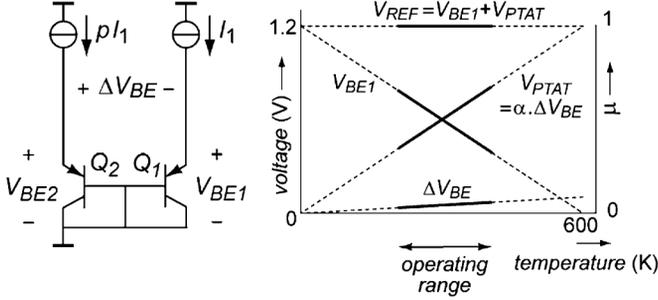
Fig. 1. Two substrate PNPs generate the required voltages (V_{PTAT} and V_{REF}) for a ratiometric temperature measurement.

Fig. 2. Nonlinear $X = V_{BE}/\Delta V_{BE}$ ($p = 5$) and linearized $\mu = \alpha/(\alpha+X)$ as a function of temperature.

its implementation. The measurement results are presented in Section V. To facilitate the comparison of the energy-efficiency of different temperature-to-digital converters, a new figure of merit (FOM) is introduced in Section VI, and the paper ends with conclusions.

II. OPERATING PRINCIPLE

In order to perform an accurate temperature to digital conversion, two well-defined signals are usually required, a temperature-dependent signal and a temperature-independent reference signal. The former is often a proportional-to-absolute-temperature (PTAT) voltage, while the latter is derived from a band-gap voltage reference. Substrate bipolar transistors have been extensively used to generate such PTAT and reference signals [4], [9]–[11].

A. The Conventional Approach

The base-emitter voltage V_{BE} of a bipolar transistor can be described as follows:

$$V_{BE} = (kT/q) \cdot \ln(I_C/I_S) \qquad (1)$$

where k is the Boltzmann constant, q is the electron charge, T is the temperature in Kelvin, I_C is the collector current and I_S is the PNP's saturation current. Due to the strong temperature dependence of the saturation current I_S, the base-emitter voltage V_{BE} exhibits a complementary-to-absolute-temperature (CTAT) behavior (see Fig. 1) with a nominal temperature coefficient (TC) of about -2 mV/K. In contrast, the base-emitter voltage *difference* of two identical bipolar transistors biased at a $1 : p$ collector current ratio is independent of I_C, I_S and is given by:

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = (kT/q) \cdot \ln(p) \qquad (2)$$

ΔV_{BE} is a PTAT voltage, which depends only on the thermal voltage kT/q and on the constant p. A linear combination of V_{BE} (CTAT) and ΔV_{BE} (PTAT) results in a band-gap reference voltage

$$V_{REF} = V_{BE} + \alpha \cdot \Delta V_{BE} \qquad (3)$$

where α is a fixed gain factor.

An analog-to-digital converter (ADC) can then be used to determine the ratio between $\alpha \cdot \Delta V_{BE}$ (PTAT) and the reference
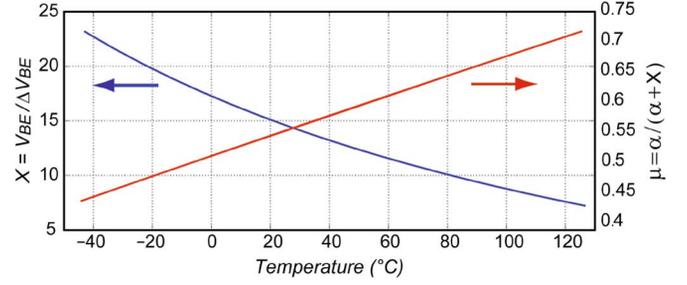
voltage V_{REF}. The digital result is a linear function of temperature:

$$\mu = \alpha \cdot \Delta V_{BE}/(V_{BE} + \alpha \cdot \Delta V_{BE}) \qquad (4)$$

A digital output D_{out} in degrees Celsius then can be found by linearly scaling the ratio μ:

$$D_{out} = \text{A} \cdot \mu - \text{B} \qquad (5)$$

where A and B are constant coefficients, A ≈ 600 and B ≈ 273 [9].

B. The Digitally-Assisted Approach

Alternatively, the ratio of V_{BE} and ΔV_{BE} can also be used as a measure of temperature [12]–[14]. This is due to the fact that all the necessary temperature information is present in V_{BE} and ΔV_{BE}. As shown in Fig. 2, for $p = 5$, the ratio $X = V_{BE}/\Delta V_{BE}$ is a nonlinear function of temperature, which ranges between 7 and 24 from $-40°C$ to $125°C$. Once X is known, however, a PTAT function μ (see Fig. 2) can be easily determined as follows:

$$\mu = \alpha \cdot \Delta V_{BE}/(V_{BE} + \alpha \cdot V_{BE}) = \alpha/(\alpha + X) \qquad (6)$$

This means that V_{BE} and ΔV_{BE} do not necessarily need to be accurately combined to generate a reference voltage V_{REF}. As a result, some of the temperature sensor's signal processing can be shifted from the analog to the digital domain, thus reducing the complexity, power consumption, and area of the analog circuitry.

Another advantage of such a digitally-assisted sensor architecture is that α is implemented in the digital domain, and is, therefore, immune to process spread. More importantly, the PTAT effect of process spread on V_{BE}, which would otherwise cause temperature-sensing errors, can be easily corrected for by adjusting α in the digital backend [12]–[14]. This is much easier to realize than analog techniques such as bias-current trimming [9], [10].

C. Block Diagram

The block diagram of the resulting smart temperature sensor is shown in Fig. 3. It consists of a zoom ADC and an analog front-end: a precision bias circuit whose PTAT output current biases the substrate PNP transistors of a bipolar core. The V_{BE} and ΔV_{BE} voltages extracted from the bipolar core are digitized by the zoom ADC, which outputs X to a digital backend,
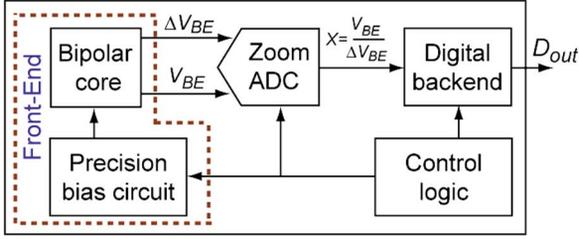
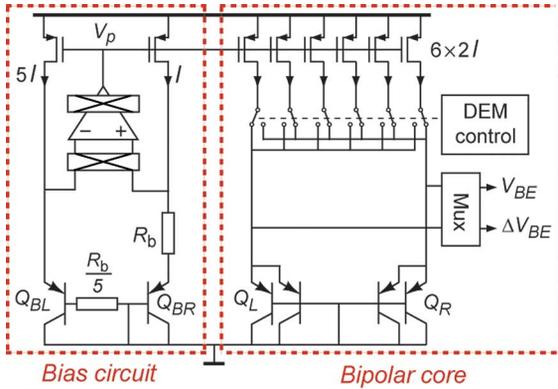Fig. 3.   Block diagram of the smart temperature sensor.

Fig. 4.   Circuit diagram of the analog front-end.

Fig. 5.   The forward current gain β_F (at 25°C) of a substrate PNP transistor (5 μm × 5 μm) as a function of collector current I_C in the 0.16 μm CMOS process used.

which, in turn, determines the PTAT function μ and D_{out}, the temperature in degrees Celsius.
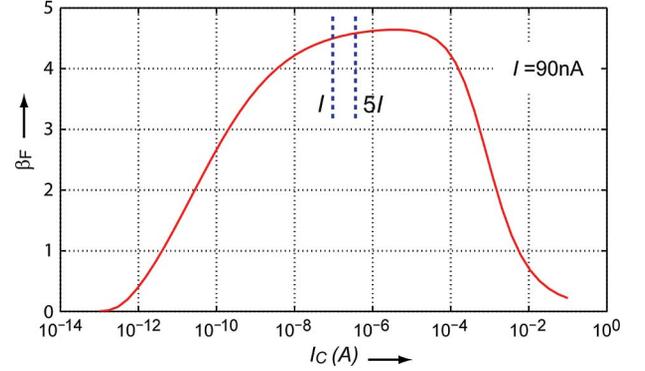
III. ANALOG FRONT-END

Fig. 4 shows the circuit diagram of the analog front-end. Although the temperature dependence of the bias current I doesn't impact the accuracy of ΔV_{BE} (see (2)), it does impact the *systematic* nonlinearity or *curvature* of V_{BE}, and hence the sensor's *systematic* error. This error decreases as the temperature dependence of the bias current I increases [8], and so a readily implementable PTAT bias current was used in this work. As shown in Fig. 4, the bias circuit uses two PNP transistors, again biased at a 5:1 current ratio, to generate an accurate PTAT current I, which is then used to bias the PNPs of the bipolar core.

A. Effect of Forward Current Gain β_F

Since a substrate PNP transistor must be biased via its emitter, the collector current and, thus, the resulting V_{BE} will depend on the transistor's current gain β_F. The spread (up to 50%) and temperature dependence of β_F will then impact the accuracy of V_{BE}. This effect becomes more significant as the current gain β_F decreases [9], as is the case in modern CMOS processes (in the 0.16 μm CMOS process used $\beta_F \sim 4.5$).

In a technique known as β_F-compensation, this problem is mitigated by modifying the PTAT bias circuit so as to generate a β_F-dependent current [9]. This is done by adding a resistor $R_b/5$ in series with the base of Q_{BL}. The opamp in the feedback loop then ensures that:

$$I = (\ln(5) \cdot (kT/q)/R_b) \cdot (\beta_F + 1)/\beta_F \qquad (7)$$

When biased with this emitter current, the collector current of the PNPs in the bipolar core (Q_L, Q_R) will be equal to $(\ln(5) \cdot (kT/q)/R_b)$, and hence their base-emitter voltages will be insensitive to variations in β_F. However, the accuracy of this technique is limited by current-mirror and β_F mismatch. Therefore, careful layout of the PNPs and the current sources is essential. A further source of V_{BE} error is the current dependency of β_F. In this design, the value of $I(= 90$ nA at 25°C) was optimized to ensure that both I and $5I$ are in a *relatively* flat part of the PNP's β_F versus collector current characteristic (see Fig. 5) [8].

B. Offset Cancellation

Besides the spread in R_b, the opamp's offset V_{OS} is a major source of bias current inaccuracy. For the temperature sensor to achieve an inaccuracy of less than $\pm0.2°$C, this offset needs to be less than 100 μV [9]. However, in CMOS, this cannot be practically achieved by transistor sizing and careful layout. Therefore, the opamp is chopped, so that the resulting bias current will be switched between $I + I_{off}$ and $I - I_{off}$ where $I_{off} = V_{OS}/R_b$. Thus, the average of the resulting V_{BE} in Q_L, Q_R will be, to first order, independent of V_{OS}. However, the use of chopping means that there will be square-wave ripple at the opamp's output V_P. While its amplitude is not important, the complete settling of V_P at the end of each chopping phase is critical, since this is the instance when the zoom ADC samples the resulting V_{BE}. Due to the large input capacitance of the current-mirror MOSFETs, a typical single-stage high-output-impedance opamp will require a relatively large bias current. In [13] for example, the opamp drew a large portion of the sensor's supply current (1.7 μA out of a total of 6 μA, or 28%).

C. Opamp Topology

As shown in Fig. 6, an adaptive self-biasing opamp [14]–[16] is used in this work. It consists of a PMOS input pair ($M_{5,6}$) with diode-connected NMOS loads ($M_{1,2}$). Since the opamp's input voltage is chopped, switch S_1 is used to maintain the correct feedback polarity. The voltage output of the input stage ($V_{gs,M1}$ or $V_{gs,M2}$) is converted into a current via M_3 and fed back to the differential pair through the $M_{10} : M_{11}$ current mirror. As a result, the tail current of the input stage is derived from its output voltage. The aspect ratio of the transistors has been chosen such
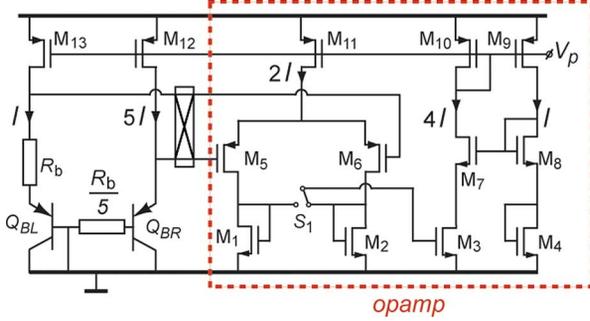
Fig. 6. Simplified circuit diagram of the bias current circuit (left hand side) and positive feedback opamp.

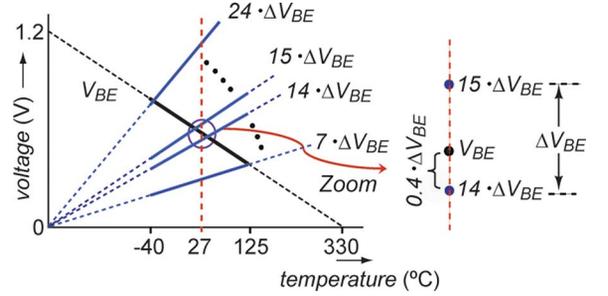
Fig. 7. Temperature dependence of $k \cdot \Delta V_{BE}$ and V_{BE} from $-40°C$ to $125°C$, e.g. at room temperature: $14 \cdot \Delta V_{BE} < V_{BE} < 15 \cdot \Delta V_{BE}$.
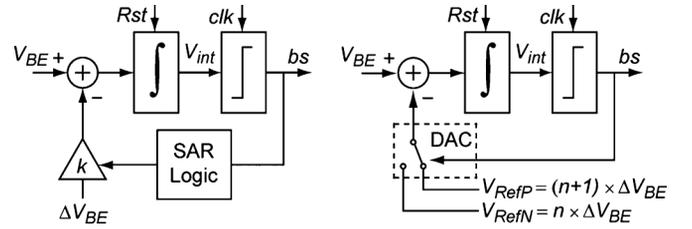

Fig. 8. Block diagram of the zoom ADC during the coarse (left) and fine (right) conversions.

that: $(W/L)_3 = 4 \cdot (W/L)_{1,2}$ and $(W/L)_{10} = 2 \cdot (W/L)_{11}$. This ensures that the current gain of the loop formed by $M_{1,2} : M_3$, $M_{10} : M_{11}$ is equal to 1 for zero input. When operated in an open-loop configuration, the positive feedback in this current loop would result in ever-increasing/decreasing output currents for negative/positive differential input voltages, corresponding to a very high DC gain. In the bias circuit, however, the amplifier is operated in a negative feedback loop which stabilizes the circuit and enforces a PTAT current I. Furthermore, since M_{10} is diode-connected, V_p is a low impedance node, which reduces the time constant associated with the settling of V_P. The opamp's bias current, therefore, can be reduced to meet the relaxed load requirements, while maintaining the gain required.

As any current mirror mismatch will result in input-referred offset, high over-drive voltages (260 mV and 130 mV for the PMOS and NMOS devices respectively, and at 25°C) and careful layout are essential. To minimize the effect of channel length modulation on the current gain of the positive feedback loop, a replica circuit drives M_8 and ensures that the V_{ds} of M_3 is equal to that of $M_{1,2}$. At 25°C, the opamp draws only 630 nA; significantly (63%) less than in our previous work [13]. The entire front-end draws only 2.1 μA from a 1.8 V supply.

D. Precision Issues

Mismatch in current sources and bipolar devices impacts the accuracy of ΔV_{BE}. Even with careful layout, a relative current ratio mismatch $\Delta p/p$ in the order of 0.1% can be expected, which, for $p = 5$, will lead to an error of about 140 mK at T = 25°C [8]. Therefore, dynamic element matching of the six current sources and two bipolar transistors in the bipolar core is essential to generate the accurate 1:5 current ratio required for an accurate ΔV_{BE} (see Fig. 4).

IV. ZOOM ADC TOPOLOGY

To minimize the temperature sensor's energy consumption, a fast, low-power ADC is required, since the bias circuit and bipolar core continue to draw current throughout a conversion. The zoom-ADC architecture combines the benefits from both SAR-ADC and 1st-order $\Sigma\Delta$ converter in a two-step conversion scheme [13], [14]. In this topology, the digital ratio $X = V_{BE}/\Delta V_{BE}$ is accurately resolved, with a high resolution and within a short conversion time.

As shown in Fig. 2, Fig. 7, the ratio $X = V_{BE}/\Delta V_{BE}$ ranges from 7 to 24 from $-40°C$ to $125°C$ $(p = 5)$. X can thus

be expressed as $X = n + \mu'$, where n and μ' are its integer and fractional parts, respectively, and can be determined separately (Fig. 8). In a coarse conversion, n is determined by a SAR algorithm, which compares V_{BE} to integer multiples of ΔV_{BE}. In a fine conversion, the fraction μ' is then determined by a 1st-order $\Delta\Sigma$ ADC, whose references are chosen so as to *zoom* into the region determined by the SAR algorithm, i.e. from $n \cdot \Delta V_{BE}$ to $(n + 1) \cdot \Delta V_{BE}$. Compared to the 200°C range of the $\Delta\Sigma$-ADCs of conventional temperature sensors, the region of interest now is quite small (less than 18°C). As a result, the resolution requirement on the $\Delta\Sigma$-ADC is greatly relaxed, leading to simple analog circuitry and short conversion times. Moreover, since the accuracy-determining fine conversion still employs a $\Delta\Sigma$-ADC, high accuracy can be obtained with the help of the usual dynamic error cancellation techniques [13], [14].

A. Implementation

As shown in Fig. 9, the zoom ADC is basically a modified 1st-order SC $\Delta\Sigma$-ADC with 24 unit sampling capacitors. At the start of each comparison step of the coarse conversion, the integrator is reset, and therefore functions as a sample-and-hold. As shown in Fig. 10, V_{BE} is then sampled on a single unit capacitor and integrated during one clock cycle. In the next clock cycle, $-\Delta V_{BE}$ is sampled on k unit capacitors and also integrated, thus a total charge proportional to $V_{BE} - k \cdot \Delta V_{BE}$ is integrated. The comparator's output bs then indicates the result of the comparison $V_{BE} > k \cdot \Delta V_{BE}$. The control logic implements the SAR algorithm, with which n can be determined within five comparison steps, since $n \leq 24$. Once n is known, the fine conversion step is determined with a $\Delta\Sigma$ charge-balancing scheme (Fig. 8). After an initial reset, the modulator operates as follows: when $bs = 0$, $(V_{BE} - n \cdot \Delta V_{BE})$ is integrated, and when $bs = 1$, $(V_{BE} - (n + 1) \cdot \Delta V_{BE})$ is in-
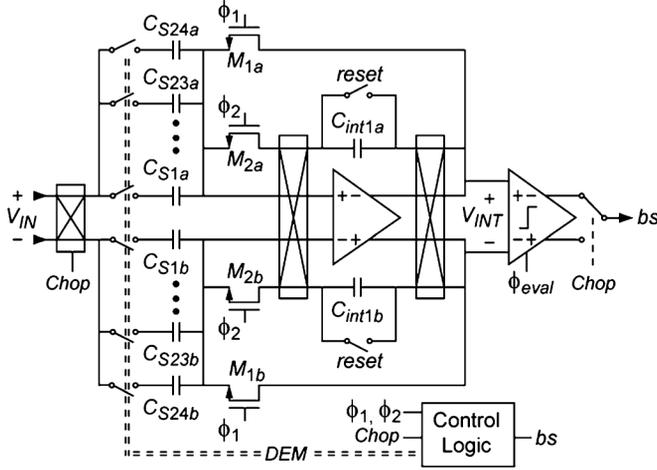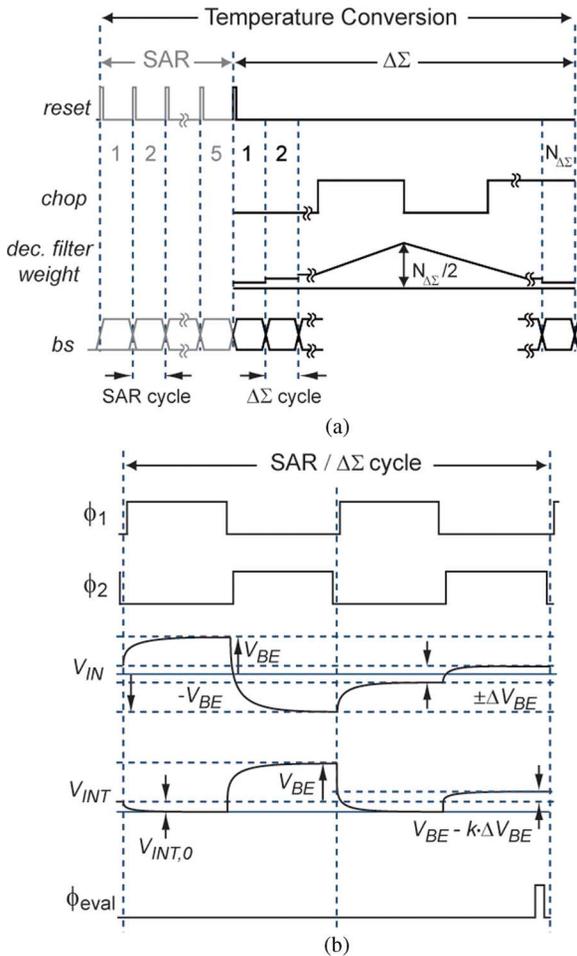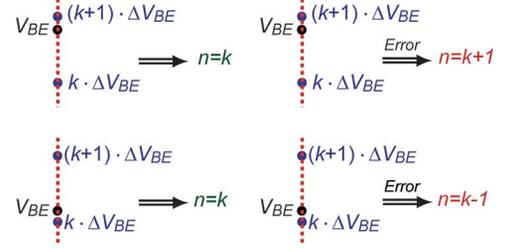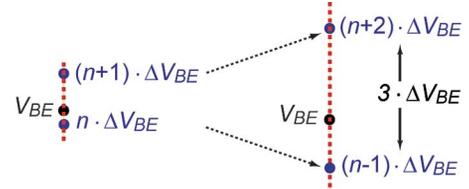
Fig. 9. Circuit diagram of the zoom ADC.

Fig. 11. Accuracy in coarse step: ideal (left) and practical (right) situations.

Fig. 12. The range is extended to $3 \cdot \Delta V_{BE}$ to avoid out-of-range errors during fine conversion step.

in Fig. 9, the main element of the zoom ADC is a SC integrator built around a folded-cascoded opamp with a gain of 86 dB. Due to the relaxed requirements on the ADC's resolution, no gain boosting is required, unlike [9], [10], thus reducing area and power. The sampling capacitors are also quite small: $C_S = 120$ fF, while the integration capacitors are $2 \cdot C_S$. The opamp's offset and $1/f$ noise are reduced by correlated double-sampling (CDS) during the coarse and fine conversions. Additionally, the entire ADC is chopped twice per fine conversion [9].

B. Accuracy in the Coarse Step

When $V_{BE} \sim k \cdot \Delta V_{BE}$, the non-idealities such as comparator offset, noise and mismatch during the coarse conversion could lead to incorrect n values, and therefore clipping in the fine conversion (see Fig. 11, right). To avoid this issue, during an extra *guard-band* cycle, the fine conversion can be appropriately extended to $3 \cdot \Delta V_{BE}$, thus relaxing the requirements on the coarse conversion [14]. As shown in Fig. 12, the range can be set-up to cover from $(n - 1) \cdot \Delta V_{BE}$ to $(n + 2) \cdot \Delta V_{BE}$, in such a way that the unknown V_{BE} is always roughly in the middle of this range, and hence avoiding the out-of-ranging in the fine conversion step.

C. Accuracy in the Fine Step

The final accuracy of zoom-ADC architecture relies on accurate references in the fine conversion step, i.e. $(n - 1) \cdot \Delta V_{BE}$ and $(n + 2) \cdot \Delta V_{BE}$ in Fig. 12. By using capacitors to realize the gain factor k, the initial accuracy of k is limited to about 0.1%, hence limiting the maximum accuracy to about 10 bits. To obtain higher accuracy levels, the capacitors are dynamically matched during the $\Delta\Sigma$ conversion step, as shown in Fig. 13.

V. Measurement Results

The temperature sensor was realized in a standard 0.16 μm CMOS process with five metal layers (Fig. 14). The chip has an active area of 0.12 mm^2, and consumes 8.2 μW from a 1.8 V

Fig. 10. (a) Timing diagram of a temperature conversion: (b) waveforms of a full SAR/$\Delta\Sigma$ cycle. V_{IN}: zoom ADC's input voltage, V_{INT}: integrator's output voltage. $V_{INT,0}$: integrator's initial voltage. k is set by the SAR logic in the coarse conversion, while $k = n$ or $n + 1$ when $bs = 0$ or 1 in the fine conversion step.

tegrated. Similar to the coarse conversion step, such integrations require two clock cycles (see Fig. 10). Since the net integrated charge is approximately zero, the bitstream average is the desired $\mu' = (V_{BE} - n \cdot \Delta V_{BE})/\Delta V_{BE}$. As illustrated
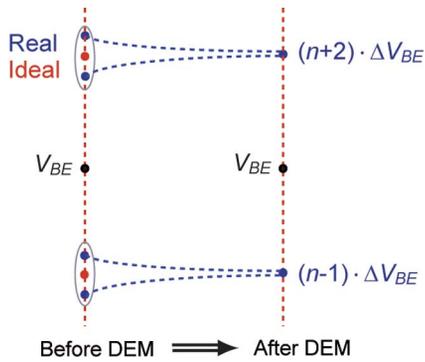
Fig. 13.   Dynamic element matching of capacitors is used to enhance the accuracy of references during the fine conversion step.

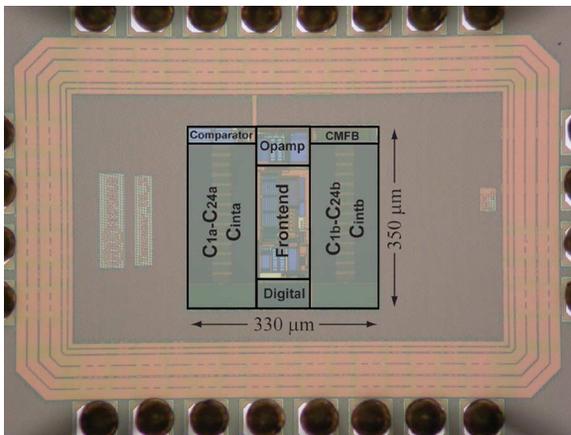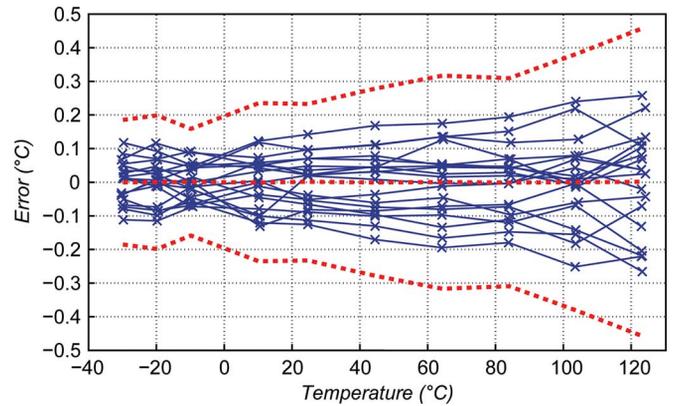Fig. 14.   Chip micrograph of the sensor.

Fig. 15.   Measured temperature error of 19 sensors before trimming; dashed lines refer to the average and $\pm 3\sigma$ limits.
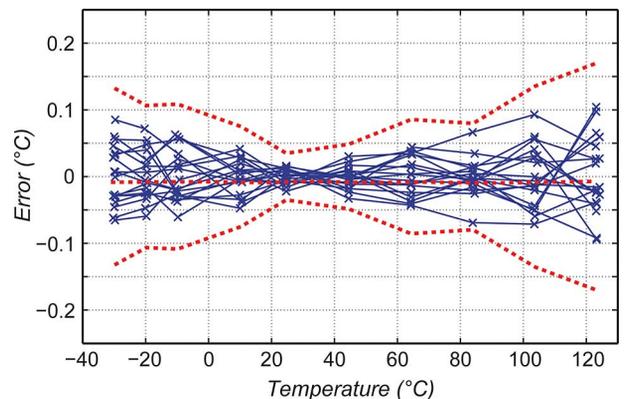

Fig. 16.   Measured temperature error of 19 sensors after digital trimming at $25°\text{C}$; dashed lines refer to the average and $\pm 3\sigma$ limits.

supply at $25°\text{C}$. The digital back-end, the control logic and the fine conversion's sinc^2 decimation filter were implemented off-chip for flexibility. For characterization, 19 devices from one batch were packaged in ceramic DIL packages and placed in a climate chamber, in good thermal contact with a platinum Pt-100 resistor calibrated to 20 mK, and were measured over the temperature range from $-30°\text{C}$ to $125°\text{C}$. As shown in Fig. 15, the resulting batch-calibrated inaccuracy was $\pm 0.5°\text{C}$ (3σ), after digital compensation for residual curvature $(\pm 0.25°\text{C})$. A single digital trim ([13], [14]) at $25°\text{C}$ was used to compensate for V_{BE}'s PTAT spread. This was done by individually tuning and embedding the α value (see (6)) for each sensor in digital back-end, thereby reducing the inaccuracy to $\pm 0.2°\text{C}$ (3σ) as shown in Fig. 16. At 10 conversions/sec (1024 $\Delta\Sigma$ cycles), the sensor achieves a kT/C limited resolution of 15 mK (rms). The sensor operates from a 1.6 V to 2 V supply with a supply sensitivity of $0.1°\text{C}/\text{V}$. The sensor's performance is summarized in Table I and compared to other low-power, state-of-the-art temperature sensors.

VI.   FIGURE OF MERIT

To facilitate the comparison of different types of smart temperature sensors, a single figure of merit (FOM) would be useful. Since a smart temperature sensor can be seen as a temperature-to-digital converter, an ADC FOM could be used, e.g. the product of energy per conversion and resolution (in Kelvin) [13], [18]. However, the sensitivity of most integrated

temperature sensors is rather low, e.g. 140 $\mu\text{V}/°\text{C}$ in this design, and so their resolution is often limited by thermal rather than quantization noise. As a result, a better FOM is the product of energy/conversion and the *square* of resolution [19]. As shown in Fig. 17, which shows the performance of several smart temperature sensors [19], this FOM usefully bounds the state-of-the-art.

In some applications, a FOM based on accuracy rather then resolution may be more appropriate. Noting that the inaccuracy of temperature sensors may be specified over different temperature ranges, *relative* inaccuracy, i.e the inaccuracy (peak-to-peak) divided by the corresponding temperature range, can be used as a normalized metric of inaccuracy. Fig. 18 shows the energy/conversion versus relative inaccuracy of several smart temperature sensors. It can be seen that an inaccuracy FOM defined as the product of energy/conversion and the *square* of relative inaccuracy also bounds the state-of-the-art [19].

As shown in Figs. 17 and 18, both the resolution and inaccuracy FOMs of this work are in line with the state-of-the-art, and are the best reported for the specific class of BJT-based temperature sensors.

VII.   CONCLUSION

A CMOS smart temperature sensor for RFID applications has been implemented in a 0.16 μm CMOS technology. It is based on the well-known bandgap principle and uses substrate PNPs

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORK

| Parameter	This work	[1]	[2]	[6]	[13]
CMOS Technology	0.16µm	0.18µm	0.18µm	0.18µm	0.16µm
Chip area	0.12mm²	0.05mm²	0.0416mm²	-	0.26mm²
Supply current †	4.6µA	220nA	193nA	30µA	6µA
Supply voltage	1.6V to 2V	1V	0.5V, 1V	1V	1.5V to 2V
Supply sensitivity	0.1°C/V	Supply referenced	-	-	0.2°C/V
Temperature range	−30° C to 125° C	0°C to 100°C	−10°C to 30°C	0°C to 100°C	−40°C to 125°C
Inaccuracy (Trim)	±0.2°C (3σ) (1-point)	-1.6°C/+3°C †† (2-point)	+1/-0.8°C †† (2-point)	+2/-2.5°C †† (1-point)	±0.25°C (3σ) (1-point)
Resolution (T_conv)	0.015°C (100msec)	0.1°C (100msec)	0.2°C (30msec)	0.04°C (7.5msec)	0.018°C (100msec)
Resolution FOM	0.17 nJ°C²	0.22 nJ°C²	0.14 nJ°C²	0.36 nJ°C²	0.29nJ°C²
Accuracy FOM	49 nJ%²	470 nJ%²	73 nJ%²	4600 nJ%²	83 nJ%²

†: At room temperature, ††: Min/Max.
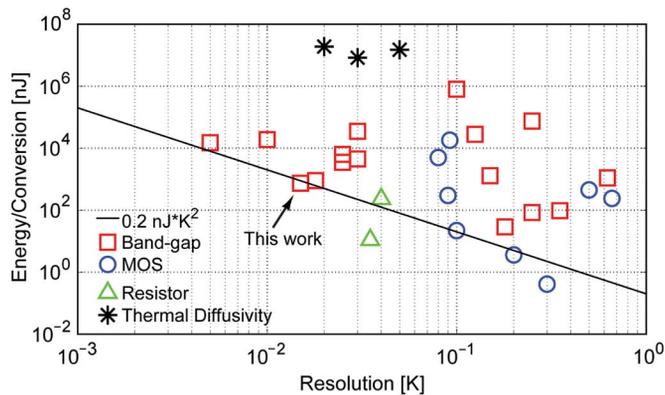
Fig. 17. Energy per conversion versus resolution for different smart temperature sensors using different sensing principles [19].
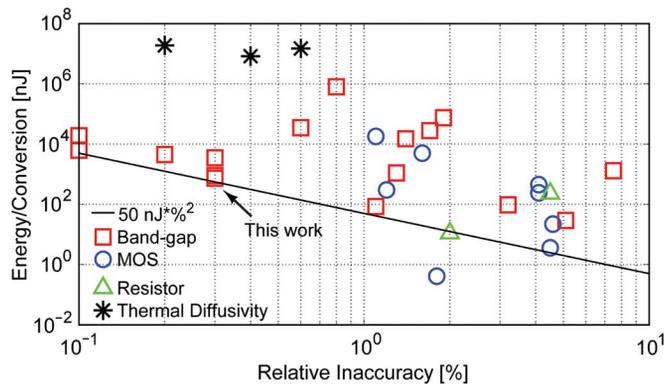

Fig. 18. Energy per conversion versus relative inaccuracy for different smart temperature sensors using different sensing principles [19].

as the main temperature-sensing elements. The use of a digitally-assisted readout architecture simplifies the analog readout circuitry considerably. Moreover, this architecture facilitates the use of digital rather than analog trimming to compensate for the sensor's main source of inaccuracy: the spread of V_{BE}. To minimize the sensor's energy consumption, a zoom ADC topology has been developed. This combines the benefits of SAR- and $\Delta\Sigma$-ADC topologies to perform an energy-efficient, high resolution, and accurate conversion. Furthermore, by using a positive feedback amplifier in the bias circuitry, the sensor's power consumption has been reduced by 24% compared to recent work [13], with no loss of accuracy. The sensor achieves an inaccuracy of $±0.2°C$ (3σ) and draws only 7.4 μW, the lowest ever reported for a precision temperature sensor.

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