A Self-Calibrated Hybrid Thermal-Diffusivity/Resistor-Based Temperature Sensor

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***Abstract*— This article describes a hybrid temperature sensor in which an accurate, but energy-inefficient, thermal diffusivity (TD) sensor is used to calibrate an inaccurate, but efficient, resistor-based sensor. The latter is based on silicided polysilicon resistors embedded in a Wien-bridge (WB) filter, while the former is based on an electrothermal filter (ETF) made from a p-diffusion/metal thermopile and an n-diffusion heater. The use of an on-chip sensor for calibration obviates the need for an external temperature reference and a temperature-stabilized environment, thus reducing the cost. To mitigate the area overhead of the TD sensor, it reuses the WB filter's readout circuitry. Realized in a 180-nm CMOS technology, the hybrid sensor occupies 0.2 mm^2. After calibration at room temperature (∼25 °C) and at an elevated temperature (∼85 °C), it achieves an inaccuracy of 0.25 °C (3σ) from −55 °C to 125 °C. The WB sensor dissipates 66 μW from a 1.8-V supply and achieves a resolution of 450 μK_{rms} in a 10-ms conversion time, which corresponds to a resolution figure-of-merit (FoM) of 0.13 pJ·K^2. The sensor also achieves a sub-10-mHz $1/f$ noise corner, which is comparable to that of bipolar junction transistor (BJT)-based temperature sensors.**

***Index Terms*— Calibration, hybrid sensor, phase-domain delta–sigma modulator (PDΔΣM), resistor-based sensor, temperature sensor, thermal diffusivity (TD).**

I. Introduction

INTEGRATED temperature sensors are widely used in many measurement and control systems. For such applications, two sensor specifications are critical: accuracy and energy efficiency. Accuracy defines the error of the resulting system, while energy efficiency defines the amount of energy needed to achieve a given resolution and is especially important in the case of battery-powered systems.

To combat process spread, integrated temperature sensors usually need calibration. This is typically done by comparing the sensor's output with that of an external reference sensor, for example, a Pt-100 thermistor. To minimize calibration error, the two sensors must reach a stable thermal equilibrium. The extra infrastructure (e.g., oil baths and ovens) and settling time needed to do this significantly increases the manufacturing cost, especially when multiple calibration temperatures are required. As a result, there is a direct tradeoff between cost and accuracy.

Most temperature sensors are based on bipolar junction transistors (BJTs) and the temperature dependency of their base–emitter voltages. With well-designed readout electronics, such sensors only require a one-point calibration to achieve inaccuracies below 0.2 °C (3σ) over a 180 °C temperature range [1]–[4]. This can be done either by temperature [1], [2] or by voltage [3], [4] calibration. The latter exploits the fact that when two BJTs are biased at a stable current density ratio, the difference in their base–emitter voltages (ΔV_{BE}) is an accurate measure of temperature. By comparing ΔV_{BE} with an external voltage reference, the die temperature can be determined with an inaccuracy of better than 0.2 °C (3σ) [4]–[6]. The use of voltage calibration obviates the need for external reference sensors and a temperature-stabilized environment, thus reducing the calibration cost. Heater-assisted voltage calibration has also been proposed [5], [6]. Here, an on-chip heater is used to elevate the die temperature above ambient, thus facilitating a rapid two-point voltage calibration, which, in turn, results in high accuracy over a wide temperature range or in the presence of the mechanical stress caused by plastic packaging.

Recently, temperature sensors based on on-chip resistors, especially silicided resistors, have been proposed [8], [9]. The latter have a large and linear temperature coefficient (TC), small $1/f$ noise, and a stable resistance. Sensors based on such resistors are typically one or two orders of magnitude more energy-efficient than BJT-based sensors [14]. However, since both the nominal resistance and TC of such resistors spread significantly, the resulting sensors require a two-point calibration to obtain BJT-like accuracy [8]–[10]. This is a significant drawback, limiting their use to applications where multi-point calibration is required anyway, such as in the frequency compensation of frequency references [7]–[10].

Thermal diffusivity (TD) sensors are another class of CMOS-compatible temperature sensors. They exploit the TD of bulk silicon, which is a well-defined function of temperature [15]. Such sensors can achieve 0.2 °C (3σ) inaccuracy over a 180 °C temperature range without individual calibration [16]. However, despite their excellent accuracy,

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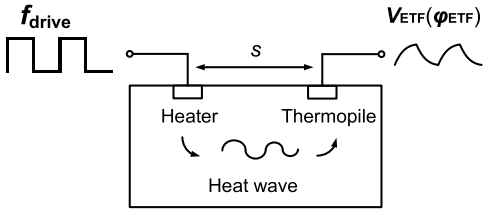
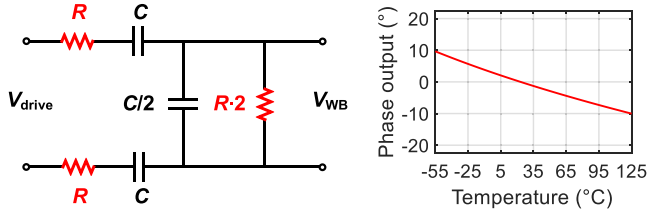


Fig. 1. TD sensor principle.



(a) (b)

Fig. 2. (a) WB front-end. (b) Calculated phase response over temperature.

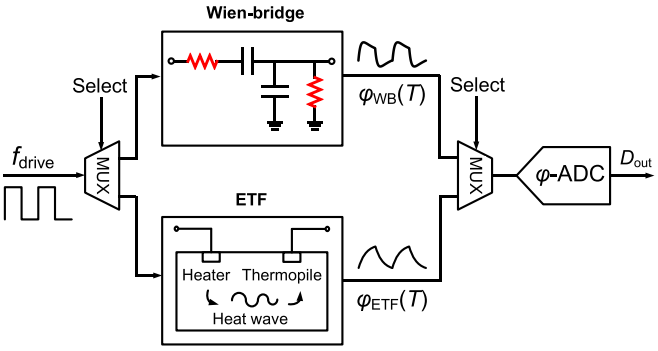


Fig. 3. Simplified structure of the hybrid sensor.

TD sensors are quite energy-inefficient, since their operation requires the injection of milliwatt-level heat pulses into the substrate.

In this article, an extended version of [18], a hybrid TD/resistor-based temperature sensor is proposed. It uses an inherently accurate TD sensor to calibrate an inaccurate, but energy-efficient, resistor-based sensor. The latter is based on silicided polysilicon resistors embedded in a Wien-bridge (WB) filter, while the former is based on an electrothermal filter (ETF) made from a p-diffusion/metal thermopile and an n-diffusion heater. When driven by an external frequency reference, both the sensors generate a temperature-dependent phase shift. As a result, their readout circuit can be shared, thus reducing the chip area and complexity.

The rest of this article is organized as follows. The sensor principles and the basic structure are described in Section II. Section III discusses the design of the resistor-based sensor based on a WB filter, as well as its readout circuits. Section IV focuses on the TD sensor design and its integration with the resistor-based sensor. The measurement results are presented in Section V, and the sensor's performance is compared with the state-of-the-art. Finally, conclusion is drawn in Section VI.

II. Sensor Principles and Basic Structure

A. TD Sensor

As shown in Fig. 1, the heart of a TD sensor is an ETF [15]. This consists of a heater and a relative temperature sensor (thermopile) realized in the substrate of a chip. When driven by a square-wave, the heater generates heat pulses, which propagate through the silicon substrate and cause temperature variations that are detected by the thermopile. Due to the finite and temperature-dependent TD of silicon D_{Si}, an ETF behaves like a low-pass filter [15]. In the case of a point heater and a point sensor, this phase shift is given by

$$\varphi_{ETF}(\omega) = -s\sqrt{\frac{\omega}{2D_{Si}}} \tag{1}$$

where D_{Si} is the TD of bulk silicon (proportional to $T^{-1.8}$) and s is the distance between the heater and the sensor. Since D_{Si} is a material property of the highly pure substrate, and s is defined by lithography, φ_{ETF} is a well-defined function of temperature and driving frequency. With a sufficiently large s (24 μm), a 3σ accuracy of 0.2 °C (3σ) over the military temperature range (−55 °C to 125 °C) can be achieved [16].

B. Resistor-Based Sensor

As shown in Fig. 2(a), the resistive sensor used in this design is a WB filter. It is a second-order bandpass filter, whose phase shift can be expressed as

$$\varphi_{WB}(\omega) = -\tan^{-1}\left(\frac{R^2C^2\omega^2 - 1}{3RC\omega}\right). \tag{2}$$

When realized from silicided polysilicon resistors (TC ∼ 0.3%/°C) and metal–insulator–metal capacitors (MIM, TC ∼ 50 ppm/°C), and driven at a constant f_{drive}, the filter's phase shift will vary by ∼20° over the military temperature range, as shown in Fig. 2(b). This phase shift can then be digitized by a phase ADC, resulting in inaccuracies of less than 0.1 °C over a 220 °C temperature range [9], after a two-point calibration.

C. Hybrid Sensor

Since the outputs of both the TD and the WB sensors are in the phase domain, a single-phase ADC can be multiplexed between them, as shown in Fig. 3, thus saving area. Since the die temperature can be assumed to be quite homogeneous, the accurate TD sensor can be used to calibrate the energy-efficient WB sensor, as will be discussed in Section V-C. After calibration, the TD sensor can be turned off to save power.

III. WB Sensor

A. Phase-Domain Delta–Sigma Modulator

As in [9], the WB sensor is read out by a phase ADC built around a phase-domain delta–sigma modulator (PD$\Delta\Sigma$M). As shown in Fig. 4(a), the WB is driven by a square wave, and its phase shift is embedded in the output current I_{WB} injected into the integrator's virtual ground. The phase demodulator is realized by chopping I_{WB} with bitstream-dependent reference phases ϕ_1 and ϕ_0. Depending on the selected phase, the demodulated current (I_{demod}) will have a positive or negative average value. The $\Delta\Sigma$M will force the loop filter's average dc

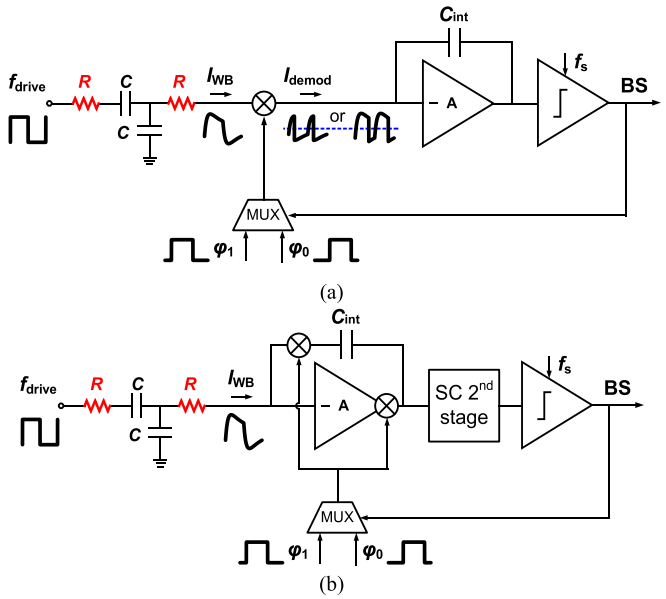


Fig. 4. (a) Simplified single-ended circuit diagram of the WB readout by a PD$\Delta\Sigma$M. (b) Circuit diagram after chopper merging and adding an SC second stage.

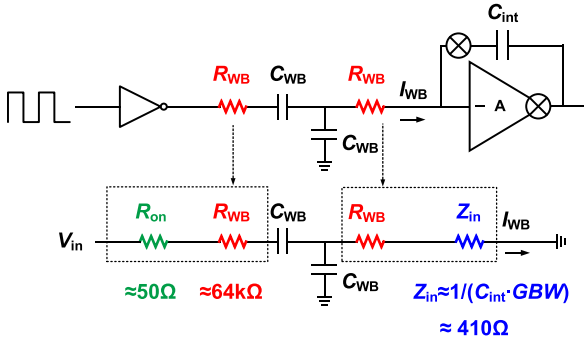


Fig. 5. Resistive error sources of the WB sensor.

input to zero, and thus the bitstream average will be a digital representation of the WB filter's phase shift.

To achieve high resolution within a short conversion time (t_{conv}), a feedforward compensated second-order $\Delta\Sigma$M is adopted. As shown in Fig. 4(b), it uses a continuous-time first stage and a discrete-time second stage for area efficiency [9]. The amplifier used in the first stage is chopped to suppress its $1/f$ noise. The required input chopper can be merged with the phase demodulator [8], thus simplifying the required control logic and minimizing errors due to charge injection mismatch.

The WB filter used in this design is inherited from [9], with $R = 64$ kΩ, $C = 5$ pF, and $f_{drive} = 500$ kHz. To accommodate RC spread over temperature and corners, a reference phase difference of 45° ($\phi_1 - \phi_0$) is chosen.

B. First-Stage Amplifier and Biasing Circuit

As shown in Fig. 5, both the ON-resistance R_{on} of the driving inverters and the input impedance of the integrator $Z_{in} \propto 1/(C_{int} \cdot \text{GBW})$ are in series with the WB and may thus limit its accuracy. In [9], the first-stage amplifier is a two-stage Miller-compensated opamp based on current-reuse stages. To maximize output swing, its output stage is realized with high-Vt transistors. It is optimized for energy efficiency and

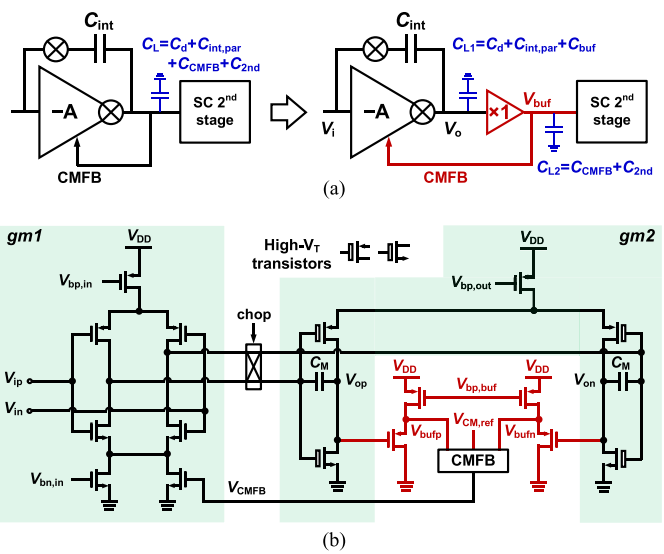


Fig. 6. (a) Loading capacitors of the first-stage amplifier with/without a buffer. (b) Two-stage amplifier and source-follower-based buffers.

achieves a GBW of ∼17 MHz. With $C_{int} = 23$ pF, this results in $Z_{in} \sim 410\ \Omega$, which is much larger than R_{on} (∼50 Ω). As a result, the variations in the opamp's GBW, for example, due to bias current spread, will limit the sensor's accuracy.

To reduce Z_{in} without increasing C_{int} (area), the GBW of the first-stage opamp should be increased. However, this should be done in a power-efficient manner. In [9], a two-stage Miller-compensated opamp is used. Its GBW is then limited by the secondary pole formed by the transconductance of its output stage (gm_2) and its load capacitor (C_L). For sufficient phase margin, the frequency of this pole (gm_2/C_L) should be 3× larger than that of the dominant pole (∼GBW), that is, $gm_2/C_L > 3 \cdot \text{GBW}$. As shown in Fig. 6(a), C_L consists of the parasitic capacitance of the integration capacitor ($C_{int,par}$), the drain capacitance of the output stage (C_d), the input capacitance seen from the common-mode feedback (CMFB) circuit (C_{CMFB}), and that of the SC-based second stage (C_{2nd}).

The first two parasitic capacitances are hard to reduce. However, the loading effect of C_{CMFB} and C_{2nd} can be removed by introducing a low-power buffer realized with PMOS source followers, as shown in Fig. 6(b). Since the second stage of the PD$\Delta\Sigma$M only processes a dc signal, the speed of the buffer is not important. It only adds ∼1.1 μA to the 16-μA supply current of the opamp in [11], as well as negligible loading capacitance. Due to the reduced capacitive load, the opamp's GBW can be doubled by adjusting the Miller capacitances.

Apart from degrading the sensor's accuracy, the presence of Z_{in} also degrades the sensor's $1/f$ noise performance. This is because Z_{in} will be modulated by the $1/f$ noise present in the opamp's bias current. To minimize this, the current mirrors of its constant-Gm biasing circuit were realized with degenerated NMOS transistors, as shown in Fig. 7. These are self-cascoded by medium-Vt devices to achieve good power supply sensitivity without using an auxiliary amplifier, as in [11].

C. System-Level Chopping

To further suppress $1/f$ noise, system-level chopping is applied to the entire sensor readout. XOR-gates are used to

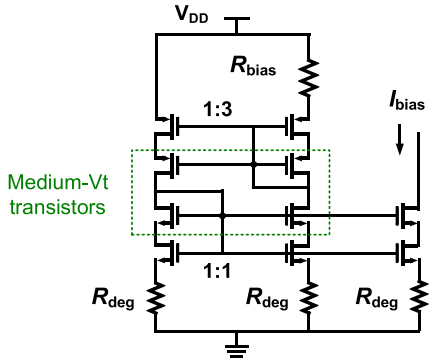


Fig. 7. Biasing generation circuit.

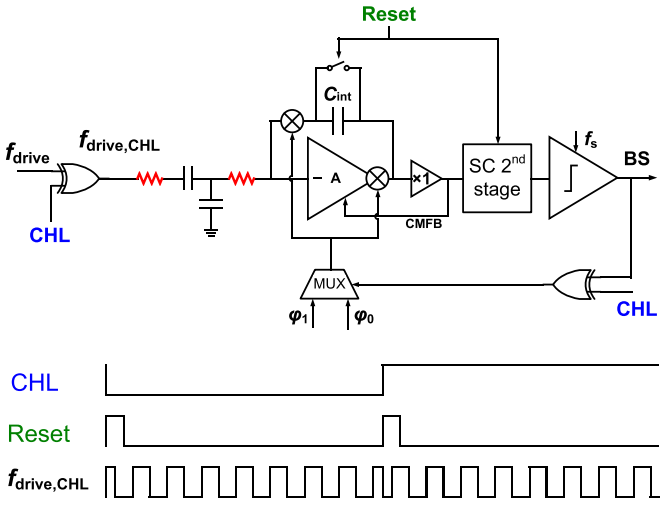


Fig. 8. System-level chopping circuits and timing diagram.

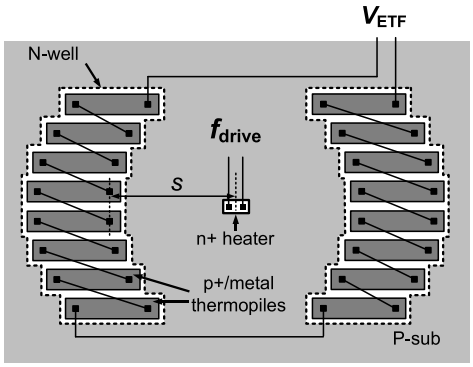


Fig. 9. ETF with a phase-contour thermopile layout [16].

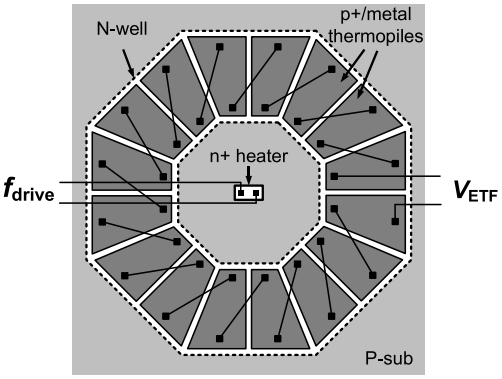


Fig. 10. ETF with an octagonal thermopile layout [17].

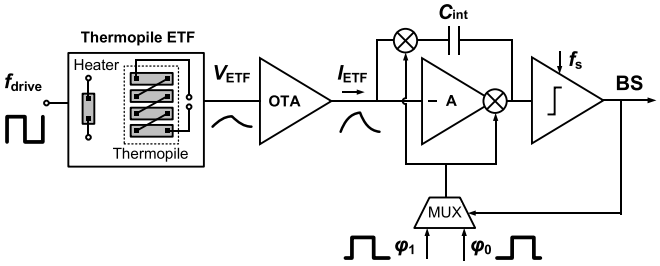


Fig. 11. Simplified single-ended circuit diagram of the ETF readout. System-level chopping and the SC second stage are not shown.

periodically invert the polarity of f_{drive} at 100 Hz (CHL). To minimize settling errors, switching is done in the middle of each half period, as shown in Fig. 8. To avoid quantization noise folding, the PD$\Delta\Sigma$M is reset at the start of each phase of system-level chopping. From simulations, the sensor's residual $1/f$ is $\sim$10 mHz and is mainly limited by the biasing circuit.

IV. TD Sensor and Integration

A. Noise-Optimized Layout

Despite achieving excellent untrimmed accuracy (0.2 °C over the military range), the TD sensor in [16] requires a relatively long conversion time ($\sim$6 s) to achieve commensurate resolution ($\sim$30 mK_{rms}), which is too long for low-cost calibration. The sensor's resolution is mainly limited by the SNR at the output of its thermopiles, whose layout is shown in Fig. 9. In this work, a polygonal thermopile layout is used, Fig. 10 [17], resulting in 5$\times$ lower thermopile resistance ($\sim$4 kΩ), and thus less noise. Furthermore, the sensor's heater power (4.2 mW) is nearly double that of [16], which proportionally increases the thermopile output ($\sim$500 μV). Together, these measures result in higher resolution ($\sim$10 mK) in a much shorter (1 s) conversion time.

B. AZed GM Stage

As shown in Fig. 11, an operational transconductance amplifier (OTA) is used to convert the output of the ETF into a current that is subsequently applied to the first integrator of a PD$\Delta\Sigma$M. In contrast to [16], the phase demodulation is now done after the OTA, as this allows the same PD$\Delta\Sigma$M to be used for both the WB and TD sensors. As a result, the OTA now needs to be fast enough to avoid adding significant phase errors to the ETF's output phase.

In this work, a telescopic OTA is used (Fig. 12). Compared with the folded-cascode OTA used in [16], it is faster and more power-efficient. It uses PMOS input transistors and resistor-degenerated NMOS current sources to ensure that its $1/f$ noise corner is lower than the intended ETF driving frequency f_{drive} ($\sim$30 kHz). Also, it has a large gm ($\sim$0.9 mS) and bandwidth ($\sim$600 MHz from simulation), which ensures that its thermal noise floor is lower than that of the ETF, and its phase delay contributes negligible phase error.

The offset of the OTA needs to be suppressed, since it will be up-modulated by the phase demodulator in the PD$\Delta\Sigma$M and the resulting ripple will limit the swing at the output of its first integrator. To suppress its offset, the OTA is auto-zeroed

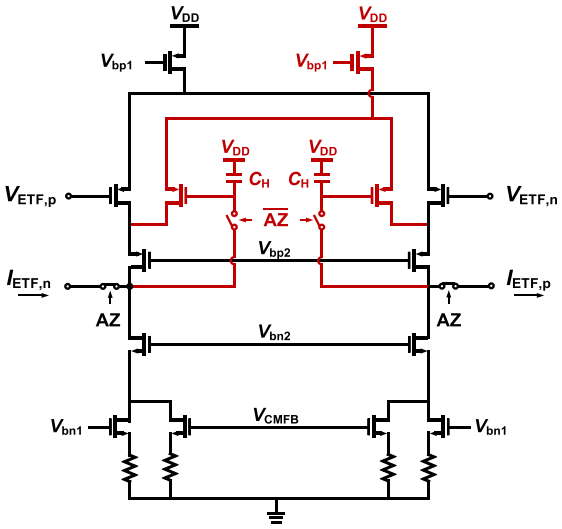


Fig. 12. Simplified schematic of the auto-zeroed OTA.

with the help of an auxiliary amplifier [Fig. 12 (red)]. This is implemented with long devices in strong inversion, resulting in a small transconductance (gm $\sim$ 0.06 mS) and a negligible contribution to the main OTA's thermal noise. Due to the use of large hold capacitors ($C_H \sim 7$ pF) and low-leakage minimum-size AZ switches, the OTA only needs to be auto-zeroed once at the start of each TD sensor conversion. The OTA consumes $\sim$500 μA from a 1.8-V supply, of which about 20% is due to the auxiliary amplifier.

C. Kelvin Connection and Integration

A multiplexer is required to connect either the WB sensor or the TD sensor to the input of the PD$\Delta\Sigma$M. A straightforward multiplexer would only involve two switches, as shown in Fig. 13(a). However, this will introduce an extra switch resistance (R_{on}) in series with the WB filter, whose spread will then degrade the filter's accuracy.

In this work, the R_{on} error is removed by Kelvin connections, as shown in Fig. 13(b). In this configuration, almost no current flows through the sense switches, while the force switches, like the chopper switches, are in the feedback loop of the first integrator. In this way, the multiplexer's switch resistance has a negligible effect on the WB filter's accuracy.

D. System Operation

Fig. 14 shows the complete circuit diagram of the hybrid sensor and the timing of signals in the TD sensor mode. To further suppress the residual offset of the AZed amplifier and the charge injection of the demodulating choppers, the entire signal path is chopped once per conversion (CHL). The AZ signal, together with the reset signal of the PD$\Delta\Sigma$M, is triggered at the start of each CHL phase (0.5 s each). To reduce its ac output during AZ, which will appear as noise, while preserving its dc output, the ETF is driven at a higher frequency ($16 \cdot f_{drive}$). The driving frequencies and phase references required by the WB and TD filters are derived from an external frequency reference by on-chip divider with a phase step of 22.5°. Different reference frequencies are used for WB/TD modes.

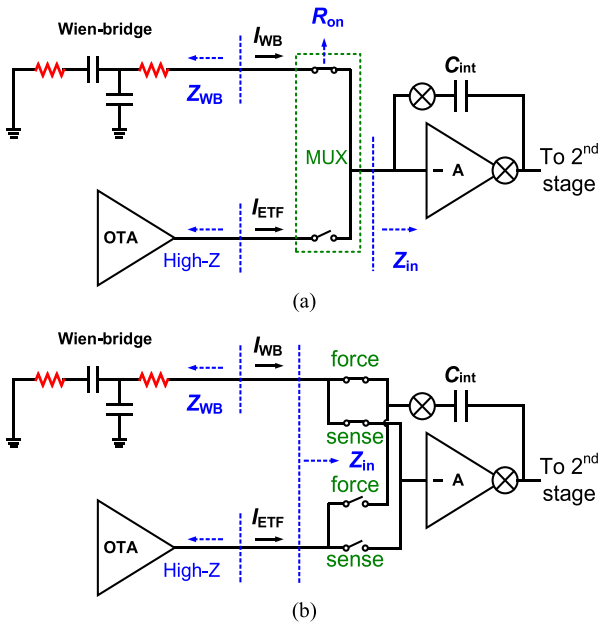


Fig. 13. Sensor integration using (a) multiplexer connection and (b) Kelvin connection.

V. Measurement Results

The sensor is fabricated in a standard 0.18-μm CMOS technology. Four hybrid sensors were implemented per die, with identical WB sensors and readout circuits but different ETF test structures. The micrograph of one sensor is shown in Fig. 15. In TD mode, each sensor consumes 5.1 mW (4.2-mW heater, 0.9-mW analog, and 0.6-μW digital) from a 1.8-V supply. In the WB mode, the heater and the OTA are turned off, and its power consumption drops to 66 μW at room temperature (RT). The sensor has an active area of 0.2 mm^2, of which $\sim$40% is occupied by the ETF and OTA. For flexibility, the decimation filters (sinc^2) are implemented off-chip. At RT, dc supply sensitivities of 0.27 °C/V (WB) and 0.4 °C/V (ETF) were observed for a supply voltage range from 1.6 to 2 V. The latter is mainly due to the sensor's self-heating.

A. Sensor Characteristic Without Calibration

Twenty samples from one wafer in ceramic dual in-line packages were characterized from -55 °C to 125 °C in a temperature-controlled oven (Vötsch VT7004). To suppress the effects of oven drift, the chips were mounted in good thermal contact with a large metal block, and a calibrated Pt-100 was used as the temperature reference.

Fig. 16 shows the ETF/WB sensor characteristic at driving frequencies of 31.25/500 kHz and phase digital-to-analog converter (DAC) ranges of [22.5°, 67.5°]/[$-$22.5°, 22.5°], respectively. Within a batch, the spread of the ETF sensor is much less than that of the WB sensor. After correcting its systematic nonlinearity (SNL) with a fixed fifth-order polynomial, the ETF sensor achieves an untrimmed inaccuracy of less than 0.2 °C (3σ) at RT, as shown in Fig. 17(a). The inaccuracy of the WB sensor is much worse, being about 10 °C (3σ).

The main sources of error in the TD sensor are expected to be self-heating and extra delay due to the limited bandwidth

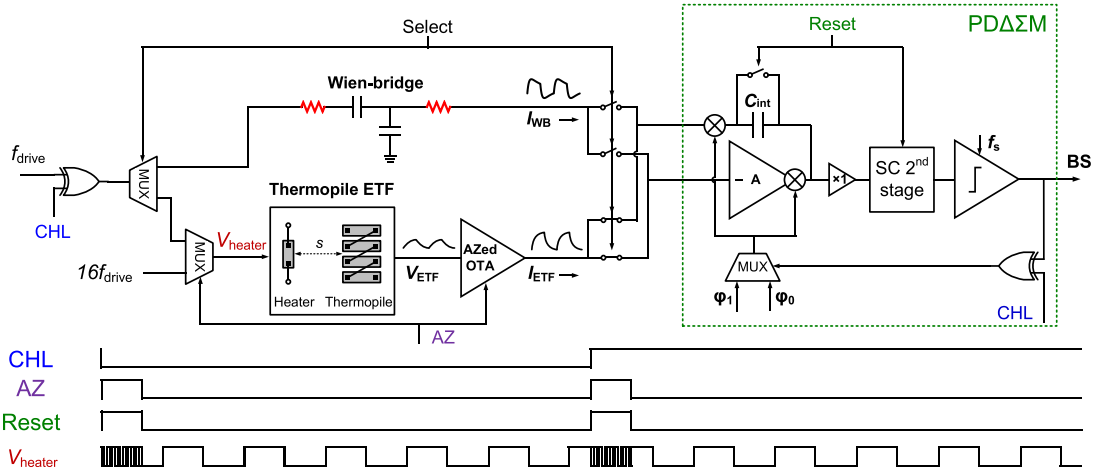


Fig. 14. Simplified circuit diagram of the hybrid sensor and its timing diagram under the TD mode.

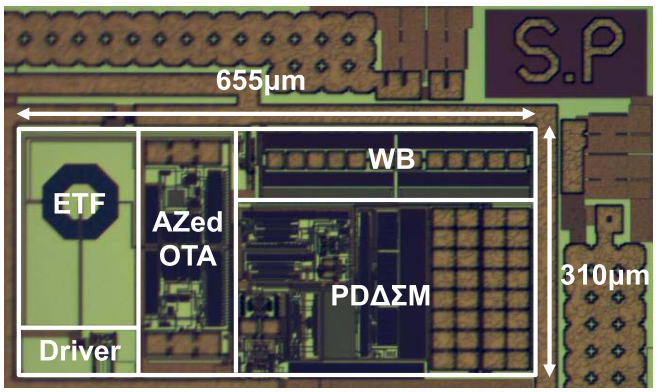


Fig. 15. Chip photograph of the fabricated sensor.

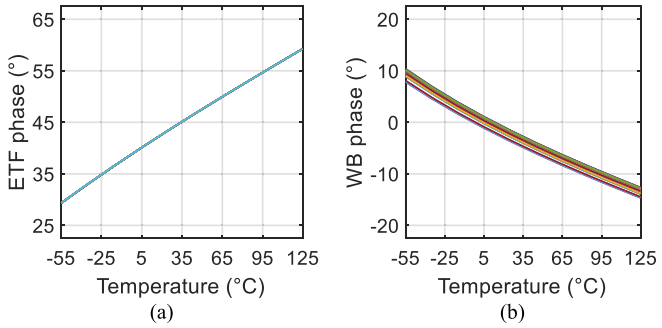


Fig. 16. Phase output characteristic of (a) TD and (b) WB temperature sensors.

of the front-end. To investigate the effect of self-heating, the heater power dissipation of all the samples (4 × 20) was measured, as shown in Fig. 18. The 3σ variation is about ~0.3 mW within a batch. Together with the estimated thermal impedance of a ceramic package (~60 °C/W), this translates into less than 0.02 °C of self-heating error. To examine the effect of electrical delay of the ETF front-end and the PDΔΣM, its driving frequency was approximately doubled (60 kHz), which would be expected to double the effect of any electrical delay. As shown in Fig. 19, although the ETF's phase sensitivity increases (by ~30%), the RT error

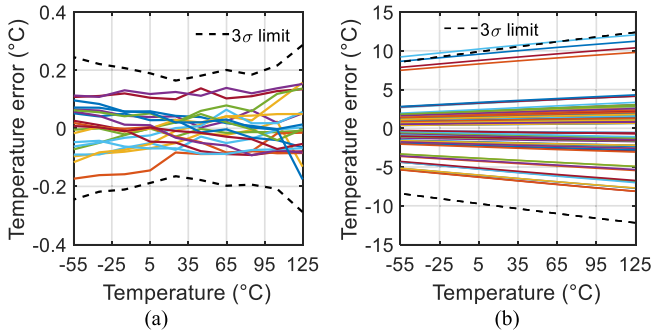


Fig. 17. Temperature error of (a) TD and (b) WB temperature sensors.

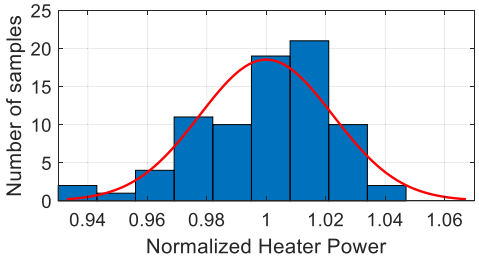


Fig. 18. Variation in heater power (all 4 × 20 ETF samples).

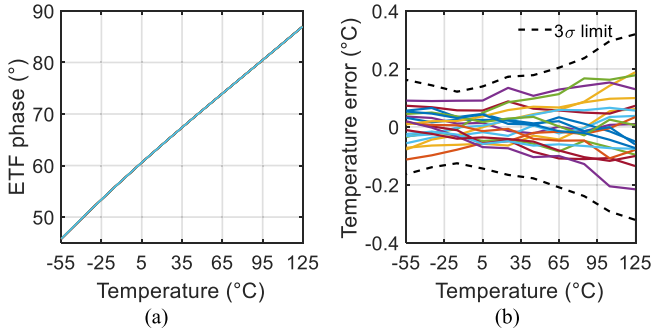


Fig. 19. (a) Phase output characteristic. (b) Temperature error of the TD sensor with f_{drive} of 60 kHz.

remains almost the same, implying that electrical delay is not a significant contributor. It should be noted that since the output amplitude of the ETF is now smaller, increasing the sensor's drive frequency actually reduces its resolution slightly.

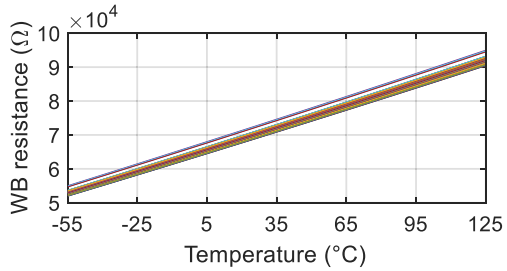


Fig. 20. Calculated resistance over temperature of the WB sensors.

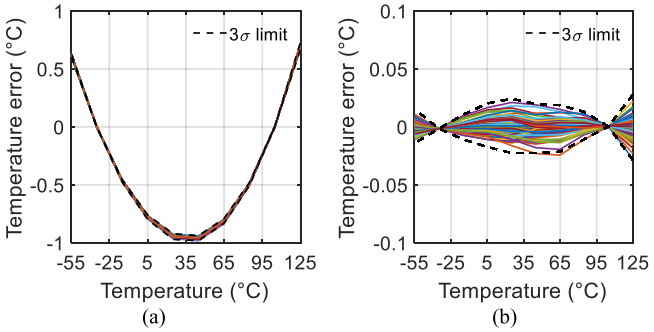


Fig. 21. WB sensor error after (a) μ-R mapping and two-point calibration and (b) μ-R mapping, two-point calibration, and systematic error removal.

B. Temperature Calibration

Traditionally, WB sensors are temperature-calibrated. To achieve the best inaccuracy after trimming, the nonlinearity of the WB and that of the PD$\Delta\Sigma$M was first removed by a fixed seventh-order polynomial that maps the bitstream average to the WB resistance (μ-R mapping), as shown in Fig. 20. As in [8] and [9], this polynomial is determined from simulation, assuming ideal PD$\Delta\Sigma$M and temperature-independent WB capacitors (5 pF). Afterward, the sensor is trimmed at -35 °C and 105 °C. As shown in Fig. 21(a), the remaining error, which is mainly due to the sensing resistor's higher order TC, is quite systematic and can be corrected by a fixed fourth-order polynomial obtained from batch calibration [8], [9]. Finally, the WB sensor achieves a 3σ error of 0.03 °C over a 180 °C temperature range, as shown in Fig. 21(b).

In a production environment, temperature calibration below RT and above 100 °C is both difficult, because the former requires a cooling system, while the latter requires either an oil bath or a temperature-controlled oven. To reduce the calibration cost, the WB sensors can be calibrated at 25 °C and 85 °C, at the expense of a slight degradation in inaccuracy: 0.05 °C (3σ), as shown in Fig. 22(a). Alternatively, a correlation-based single-point calibration [8] can be used. Unfortunately, this results in much worse inaccuracy: ~0.5 °C (3σ) over the same temperature range, as shown in Fig. 22(b).

C. Self-Calibration

For self-calibration, the TD sensor is used to calibrate the WB sensor. Since both the sensors are on the same die and thus are at the same temperature, the strict temperature settling requirement of traditional temperature calibration can be greatly relaxed. In fact, the temperature at which the sensor is calibrated does not need to be well-defined.

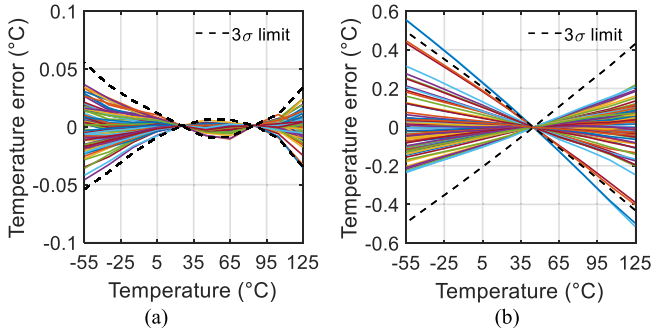


Fig. 22. WB sensor error after (a) two-point calibration at 25 °C and 85 °C and (b) one-point calibration at 45 °C.

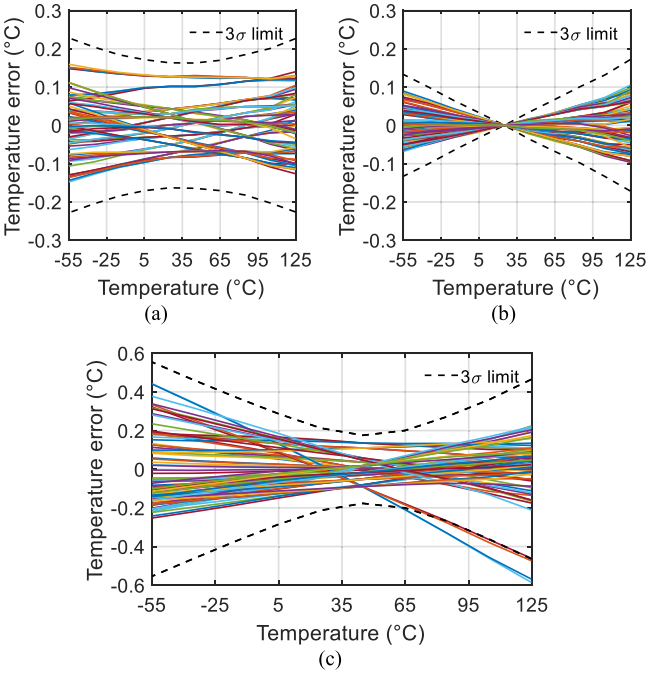


Fig. 23. WB sensor error after (a) two-point self-calibration at 25 °C and 85 °C, (b) 1-pt trim at 25 °C and a 1-pt self-calibration at 85 °C, and (c) 1-pt self-calibration at 45 °C.

To minimize calibration time, the WB/TD sensors are first read out at room temperature, and then at an elevated temperature (~85 °C). This results in a WB inaccuracy of 0.25 °C (3σ), as shown in Fig. 23(a).

As a compromise between calibration cost and accuracy, the hybrid sensor could be temperature-calibrated at RT, which allows the TD sensor to be offset-trimmed before it is used to calibrate the WB sensor at an elevated temperature. Compared with normal two-point temperature calibration, this method only requires a temperature-stabilized environment at RT, which is easier to achieve. The result is a somewhat improved WB inaccuracy of 0.15 °C, as shown in Fig. 23(b). With only a one-point self-calibration, an inaccuracy of 0.6 °C is achieved, which is slightly worse than obtained with a one-point temperature calibration, as shown in Fig. 23(c).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ART

	van Vroonhoven ISSCC'10 [16]	Souri JSSC'13 [4]	Yousefzadeh ISSCC'17 [5]	Pan JSSC'18 [8]	Pan ISSCC'19 [9]	**This work**	
Sensor type	Thermal diffusion	BJT	BJT	Resistor WB	Resistor WB	**Thermal diffusion**	**Resistor WB**
CMOS Technology	0.18µm	0.16µm	0.16µm	0.18µm	0.18µm	**0.18µm**	
Area (mm^2)	0.18	0.08	0.17	0.72	0.12	**0.20**	
Temperature range	−55°C to 125°C	−55°C to 125°C	−55°C to 125°C	−40°C to 85°C	−40°C to 180°C	**−15°C to 105°C**	**−55°C to 125°C**
3σ inaccuracy (°C) (Temp. trimming points [a])	0.2	0.15 [b]	0.3 [b]	0.03 (2)	0.1 (2)	**0.2**	**0.25** / **0.03 (2)**
$1/f$ noise corner (Hz)	--	--	--	<1	~1	**--**	**<0.01**
Power (mW)	3	0.005	0.007	0.16	0.052	**5.1**	**0.066**
Conversion time (ms)	6250	5.3	5	5	10	**1000**	**10**
Resolution (mK)	20	20	15	0.41	0.46	**15**	**0.45**
Resolution FoM (pJ·K^2) [c]	7.5×10^6	11	7.8	0.13	0.11	**1.2×10^6**	**0.13**

[a] Trimming points that require accurate temperature information. [b] Requires a voltage reference. [c] FoM = Energy / Conversion × (Resolution)^2.

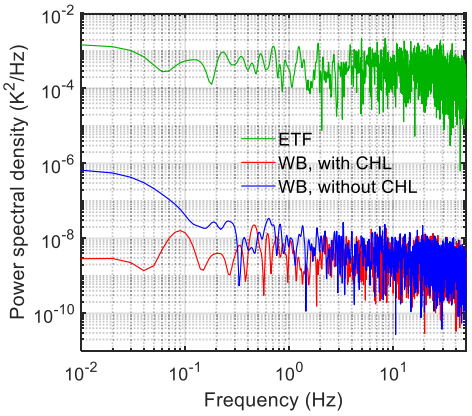


Fig. 24. Noise power spectral densities of the WB and TD sensors.

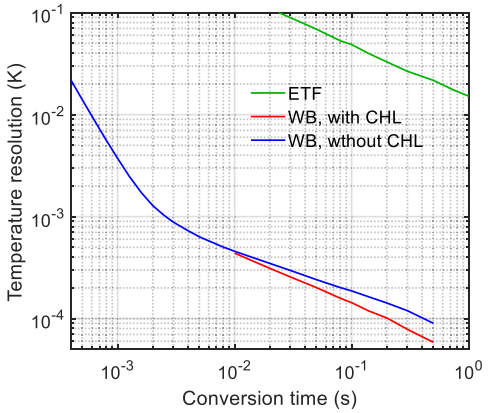


Fig. 25. Resolution versus conversion time of different sensors.

D. Resolution and FoM

After decimated by sinc^2 filters, the sensors' power spectral densities (100-s interval, Hanning window, 3× averaging) are shown in Fig. 24, and the corresponding resolution versus conversion time plots are shown in Fig. 25. To accurately determine the WB sensor resolution, a differential measurement is used, that is, it is calculated from the standard deviation of the output difference between two identical sensors on the same die. The WB sensor achieves 450 μK_{rms} resolution with $T_{conv} = 10$ ms with a 1-s interval, which corresponds to a 0.13-pJ·K^2 resolution figure-of-merit (FoM). After enabling system-level chopping ($f_{CHL} = 100$ Hz), its $1/f$ noise corner drops from ~1 Hz to below 10 mHz. In comparison, the TD sensor's resolution is only 15 mK with $T_{conv} = 1$ s and $f_{CHL} = 1$ Hz, which corresponds to a resolution FoM of 1.2 μJ·K^2.

E. Comparison to Previous Work

Table I summarizes the performance of the proposed hybrid sensor prototype and compares it with previous WB sensors [8], [9] as well as other sensors with low-cost calibration (BJT [4], [5] or TD [16]). Compared with previous WB sensors, this work achieves a state-of-the-art relative inaccuracy after a 2-pt temperature calibration and the lowest reported $1/f$ noise corner, while the resolution FoM remains roughly the same. After a cost-effective heating-assisted self-calibration that does not require accurate temperature information, this sensor achieves an inaccuracy of 0.25 °C from −55 °C to 125 °C (3σ), which is comparable to that of the voltage-calibrated BJT sensors. Although slightly less accurate than the state-of-the-art TD sensor [16], this sensor is 6× more energy-efficient. More importantly, it can achieve sufficient resolution for self-calibration with a short conversion time of 1 s. It is also worth noting that this work serves as a prototype of the TD/resistor hybrid temperature sensor. Due to the scalability of TD sensors, better performance can be expected in nanometer CMOS processes.

VI. CONCLUSION

A hybrid TD/resistor-based temperature sensor has been realized in a standard 0.18-μm CMOS technology. By self-calibrating an inaccurate, but energy-efficient, resistor-based sensor using an inherently accurate, but power-hungry, TD sensor, the hybrid sensor achieves both high energy efficiency and decent accuracy. As the need for external references and temperature-stabilized environments is obviated by the use of an on-chip reference, calibration time and costs can be greatly reduced. Also, the chip area overhead

is suppressed by reusing the PD$\Delta\Sigma$M readout circuit. The sensor dissipates 66 μW from a 1.8-V supply and achieves an inaccuracy of 0.25 °C (3σ) from -55 °C to 125 °C after self-calibration at room temperature (RT, $\sim$25 °C) and an elevated temperature ($\sim$85 °C). It also achieves a sub-10-mHz $1/f$ noise corner and a resolution FoM of 0.13 pJ·K^2.

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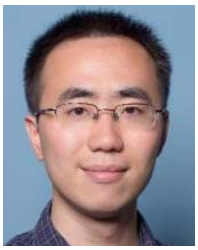

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